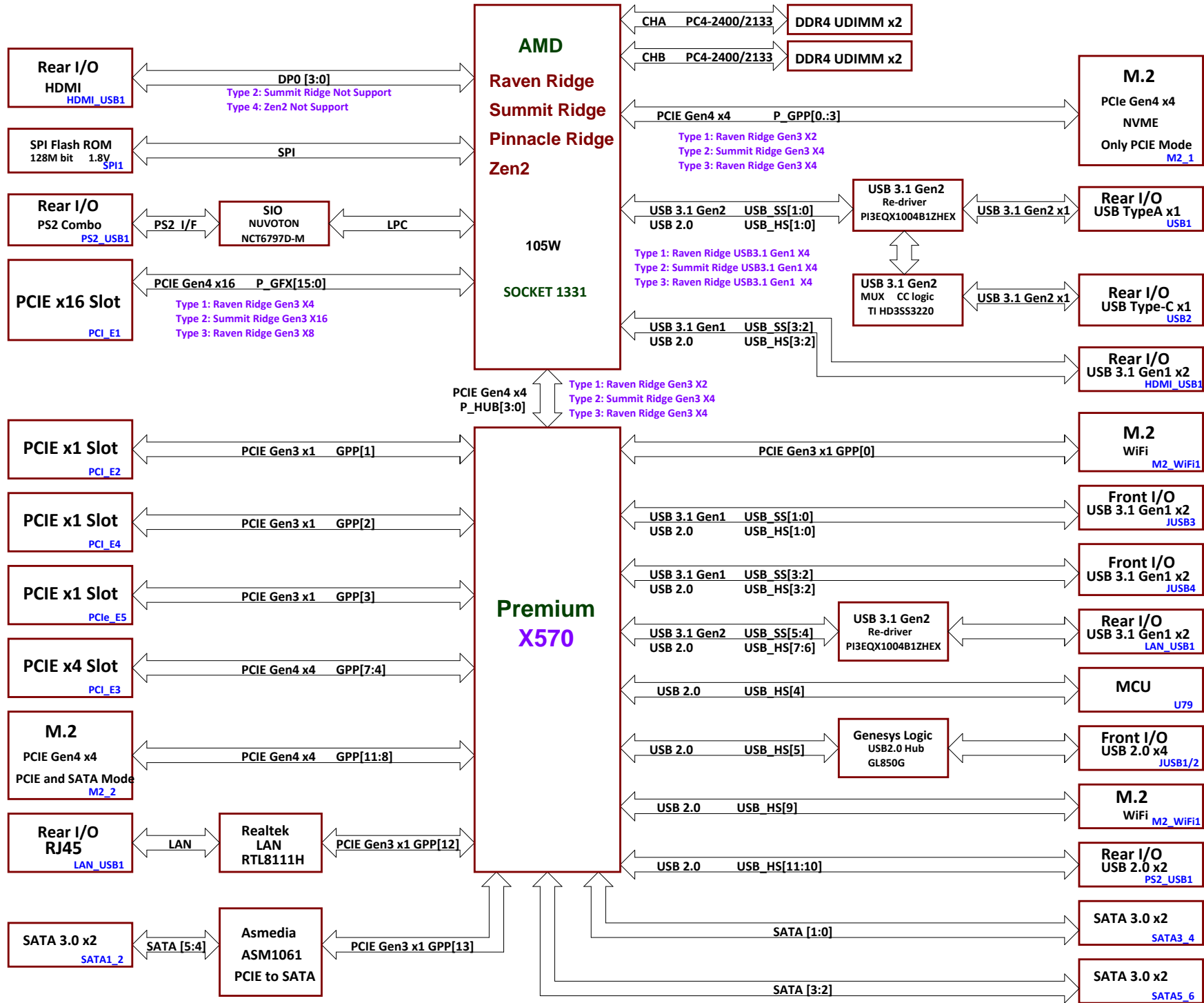
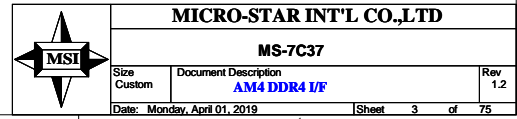


AMD AM4

GAMING EDGE AC

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TYPE	PCIE	SATA
TYPE 0/1	2	2
TYPE 2/3/4	2 or 4	2 or 0

PCI_E1 X16
(For Type-2/4)

Type1 Not Supported GFX 4~15

Type3 Not Support GFX 8~15

(15) APU_RXP0 >>> AE8 P_HUB_RXP[0]
(15) APU_RXN0 >>> AD8 P_HUB_RXN[0]
(15) APU_RXP1 >>> AB8 P_HUB_RXP[1]
(15) APU_RXN1 >>> AA8 P_HUB_RXN[1]
(15) APU_RXP2 >>> Y8 P_HUB_RXP[2]
(15) APU_RXN2 >>> Y7 P_HUB_RXN[2]
(15) APU_RXP3 >>> W4 P_HUB_RXP[3]
(15) APU_RXN3 >>> W5 P_HUB_RXN[3]

(25) APU_GPP_RXP0 >>> AR9 P_GPP_RXP[0]
(25) APU_GPP_RXN0 >>> AT9 P_GPP_RXN[0]
(25) APU_GPP_RXP1 >>> AM9 P_GPP_RXP[1]
(25) APU_GPP_RXN1 >>> AM10 P_GPP_RXN[1]
(25) APU_GPP_RXP2 >>> AR10 P_GPP_RXP[2]
(25) APU_GPP_RXN2 >>> AP10 P_GPP_RXN[2]
(25) APU_GPP_RXP3 >>> AP11 P_GPP_RXP[3]
(25) APU_GPP_RXN3 >>> AN11 P_GPP_RXN[3]

(20) GFX_RXP0 >>> F6 P_GFX_RXP[0]
(20) GFX_RXN0 >>> F5 P_GFX_RXN[0]
(20) GFX_RXP1 >>> G5 P_GFX_RXP[1]
(20) GFX_RXN1 >>> G4 P_GFX_RXN[1]
(20) GFX_RXP2 >>> H7 P_GFX_RXP[2]
(20) GFX_RXN2 >>> H6 P_GFX_RXN[2]
(20) GFX_RXP3 >>> J6 P_GFX_RXP[3]
(20) GFX_RXN3 >>> J5 P_GFX_RXN[3]
(20) GFX_RXP4 >>> K8 P_GFX_RXP[4]
(20) GFX_RXN4 >>> K7 P_GFX_RXN[4]
(20) GFX_RXP5 >>> K5 P_GFX_RXP[5]
(20) GFX_RXN5 >>> K4 P_GFX_RXN[5]
(20) GFX_RXP6 >>> L7 P_GFX_RXP[6]
(20) GFX_RXN6 >>> L6 P_GFX_RXN[6]
(20) GFX_RXP7 >>> M6 P_GFX_RXP[7]
(20) GFX_RXN7 >>> M5 P_GFX_RXN[7]
(20) GFX_RXP8 >>> N8 P_GFX_RXP[8]
(20) GFX_RXN8 >>> N7 P_GFX_RXN[8]
(20) GFX_RXP9 >>> N5 P_GFX_RXP[9]
(20) GFX_RXN9 >>> N4 P_GFX_RXN[9]
(20) GFX_RXP10 >>> P7 P_GFX_RXP[10]
(20) GFX_RXN10 >>> P6 P_GFX_RXN[10]
(20) GFX_RXP11 >>> R6 P_GFX_RXP[11]
(20) GFX_RXN11 >>> R5 P_GFX_RXN[11]
(20) GFX_RXP12 >>> T8 P_GFX_RXP[12]
(20) GFX_RXN12 >>> T7 P_GFX_RXN[12]
(20) GFX_RXP13 >>> T4 P_GFX_RXP[13]
(20) GFX_RXN13 >>> T5 P_GFX_RXN[13]
(20) GFX_RXP14 >>> U7 P_GFX_RXP[14]
(20) GFX_RXN14 >>> U6 P_GFX_RXN[14]
(20) GFX_RXP15 >>> V6 P_GFX_RXP[15]
(20) GFX_RXN15 >>> V5 P_GFX_RXN[15]

Within 1500 mils from APU

Within 1000 mils from APU

W8 P_ZVDDP Type0 Only
W9 SATA_ZVDDP Type0 Only

AM4
PART 3 OF 9

N42-331A030-L06

PCIE

SATA Express

P_HUB_TXP[0] >>> AE4 APUTXP0 C831 0.22u10X4
P_HUB_TXN[0] >>> AE5 APUTXN0 C832 0.22u10X4
P_HUB_TXP[1] >>> AA5 APUTXP1 C800 0.22u10X4
P_HUB_TXN[1] >>> AB5 APUTXN1 C801 0.22u10X4
P_HUB_TXP[2] >>> AC6 APUTXP2 C815 0.22u10X4
P_HUB_TXN[2] >>> AC7 APUTXN2 C816 0.22u10X4
P_HUB_TXP[3] >>> AD5 APUTXP3 C802 0.22u10X4
P_HUB_TXN[3] >>> AD6 APUTXN3 C803 0.22u10X4

P_GPP_TXP[0] >>> AT12 APU_GPP_TXP0 (25)
P_GPP_TXN[0] >>> AR12 APU_GPP_TXN0 (25)
P_GPP_TXP[1] >>> AP13 APU_GPP_TXP1 (25)
P_GPP_TXN[1] >>> AR13 APU_GPP_TXN1 (25)
P_GPP_TXP[2] >>> AL13 APU_GPP_TXP2 (25)
P_GPP_TXN[2] >>> AM13 APU_GPP_TXN2 (25)
P_GPP_TXP[3] >>> AN14 APU_GPP_TXP3 (25)
P_GPP_TXN[3] >>> AP14 APU_GPP_TXN3 (25)

SATA 1 supported M.2 SATA mode

D1 >>> GFX_TXP0 (20)
E1 >>> GFX_TXN0 (20)
E3 >>> GFX_TXP1 (20)
F3 >>> GFX_TXN1 (20)
F2 >>> GFX_TXP2 (20)
G2 >>> GFX_TXN2 (20)
G1 >>> GFX_TXP3 (20)
H1 >>> GFX_TXN3 (20)
H3 >>> GFX_TXP4 (20)
J3 >>> GFX_TXN4 (20)
J2 >>> GFX_TXP5 (20)
K2 >>> GFX_TXN5 (20)
K1 >>> GFX_TXP6 (20)
L1 >>> GFX_TXN6 (20)
L3 >>> GFX_TXP7 (20)
M3 >>> GFX_TXN7 (20)
M2 >>> GFX_TXP8 (20)
N2 >>> GFX_TXN8 (20)
N1 >>> GFX_TXP9 (20)
P1 >>> GFX_TXN9 (20)
P3 >>> GFX_TXP10 (20)
R3 >>> GFX_TXN10 (20)
R2 >>> GFX_TXP11 (20)
T2 >>> GFX_TXN11 (20)
T1 >>> GFX_TXP12 (20)
U1 >>> GFX_TXN12 (20)
U3 >>> GFX_TXP13 (20)
V3 >>> GFX_TXN13 (20)
V2 >>> GFX_TXP14 (20)
W2 >>> GFX_TXN14 (20)
W1 >>> GFX_TXP15 (20)
Y1 >>> GFX_TXN15 (20)

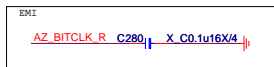
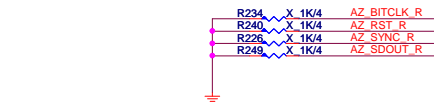
PCI_E1 X16
(For Type-2/4)

Type1 Not Supported GFX 4~15

Type3 Not Support GFX 8~15

Within 1500 mils from APU
Within 1500 mils from APU
Within 1000 mils from APU
Within 1000 mils from APU

MSI			
MICRO-STAR INT'L CO.,LTD			
MS-7C37			
Size Custom	Document Description		Rev 1.2
AM4 PCIE / SATAE			
Date: Monday, April 01, 2019		Sheet 4 of 75	



CPU_1P8_S5

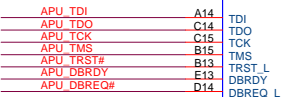
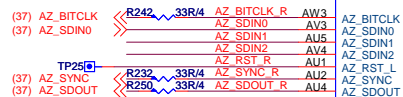


3VSB



For Debug1

For Debug2



CPU1D



AUDIO

DISPLAY-0

DISPLAY-1

TEST

DISPLAY-2

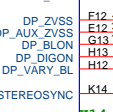
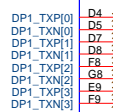
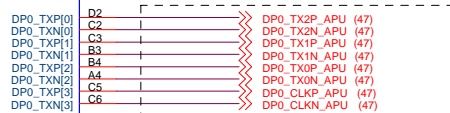
AM4

PART 4 OF 9

N12-331A030-L06

ZIF-SOCKET1331

For HDMI



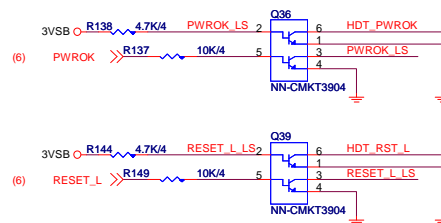
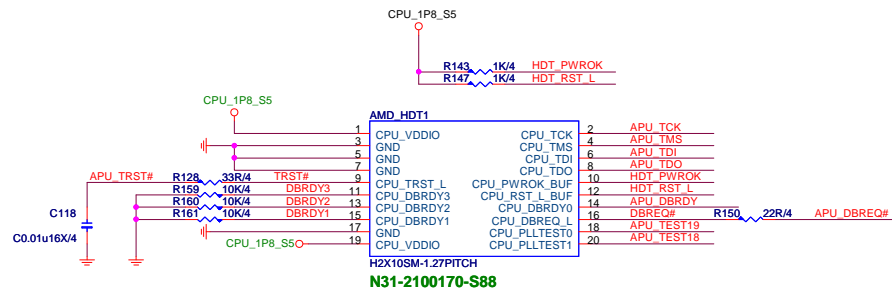
K14 PIN: 有HDMI SPEC的話請Pull-up
ENABLE功能

Not supported on TYPE 2/4

Type0 Only

For Debug2

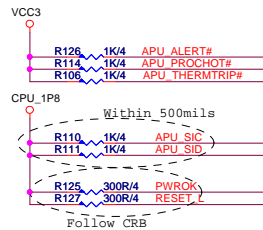
Not support Type2



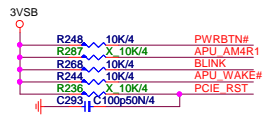
MICRO-STAR INT'L CO.,LTD

MS-7C37

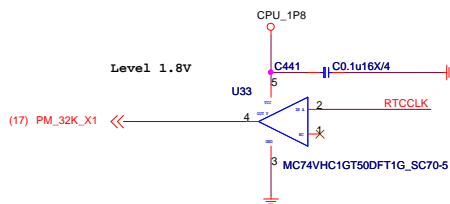
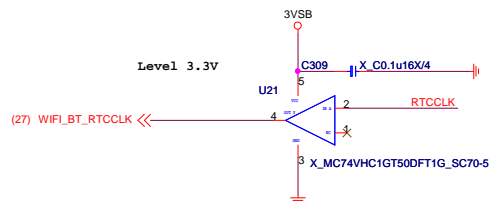
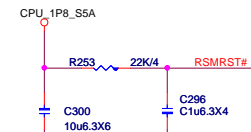
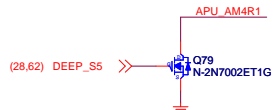
Size	Document Description	Rev
Custom	AM4 Display / Audio	1.2
Date:	Monday, April 01, 2019	Sheet 5 of 75



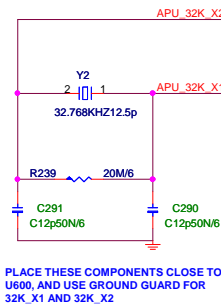
Add for HDT and
close to PIN E16 & B16



Turn off power when
BIOS into deep mode

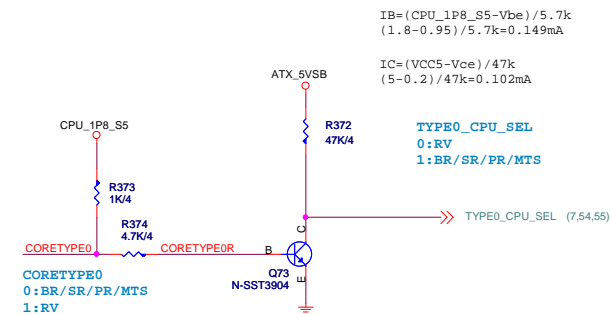


Layout: Place x'tal within 1.5 inch of APU



PLACE THESE COMPONENTS CLOSE TO
U600, AND USE GROUND GUARD FOR
32K_X1 AND 32K_X2

AM4 CPU TYPE Circuit



$$I_B = (CPU_1P8_S5 - V_{be}) / 5.7k$$

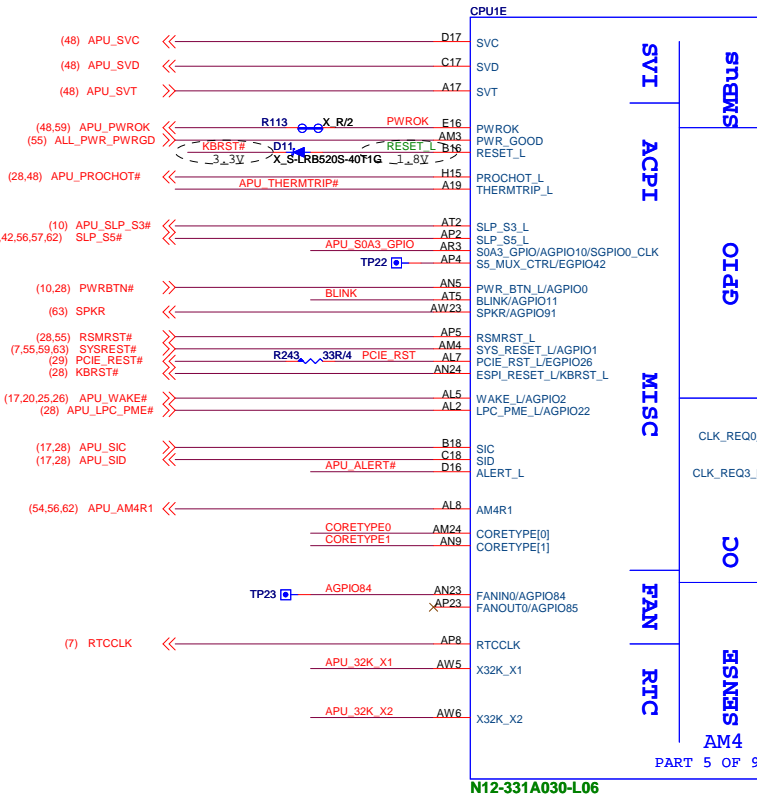
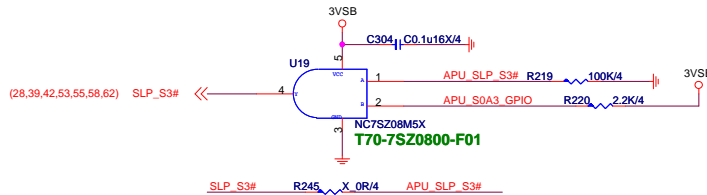
$$(1.8 - 0.95) / 5.7k = 0.149mA$$

$$I_C = (VCC5 - V_{ce}) / 47k$$

$$(5 - 0.2) / 47k = 0.102mA$$

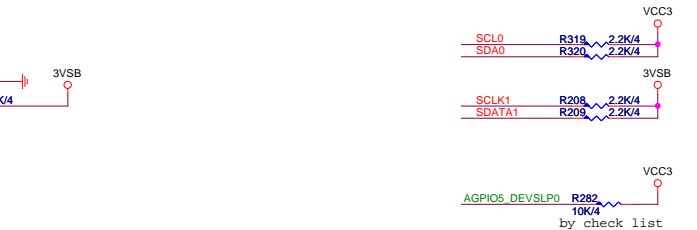
TYPE0_CPU_SEL
0:RV
1:BR/SR/PR/MTS

TYPE0_CPU_SEL (7,54,55)



N12-331A030-L06

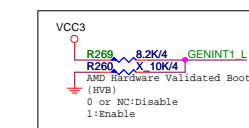
PART 5 OF 9



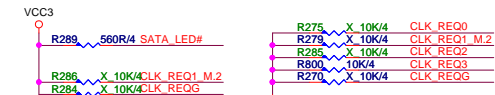
AGPIO5_DEVSLP0 R282 10K/4
by check list

For CNTL M.2 PCIE or SATA

For Select Auto or Manual



GPIO97-100 for Debug LED



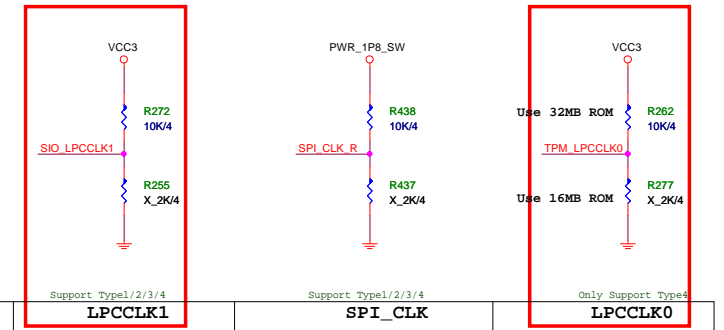
SPEC no Support

CPU	TYPE	CORETYPE 1	CORETYPE 0
BR	0	0	0
NA		0	1
SR	2	1	0
RV/ZP	3	1	1
MTS	4	1	1

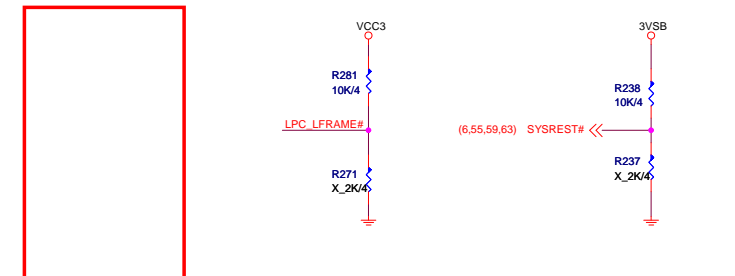


MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size	Document Description	Rev
Custom	AM4 SVI/ACPI/GPIO	1.2
Date:	Monday, April 01, 2019	Sheet 6 of 75

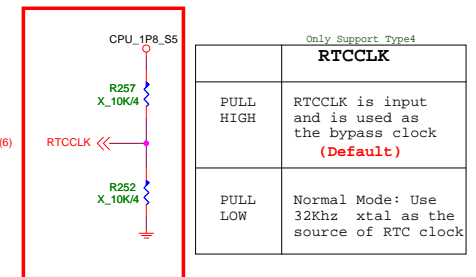
Strapping Options



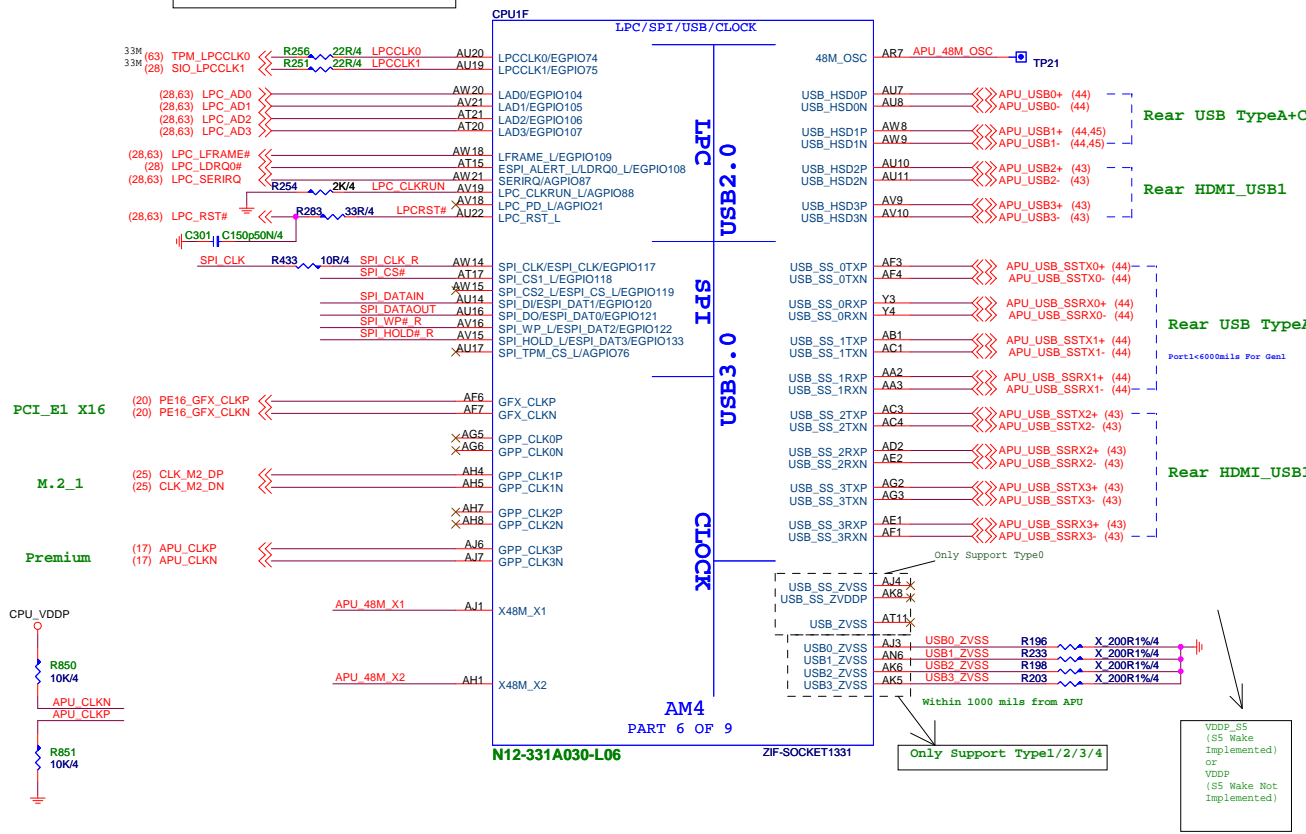
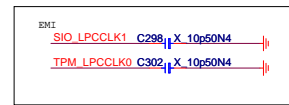
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image (Default)
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]



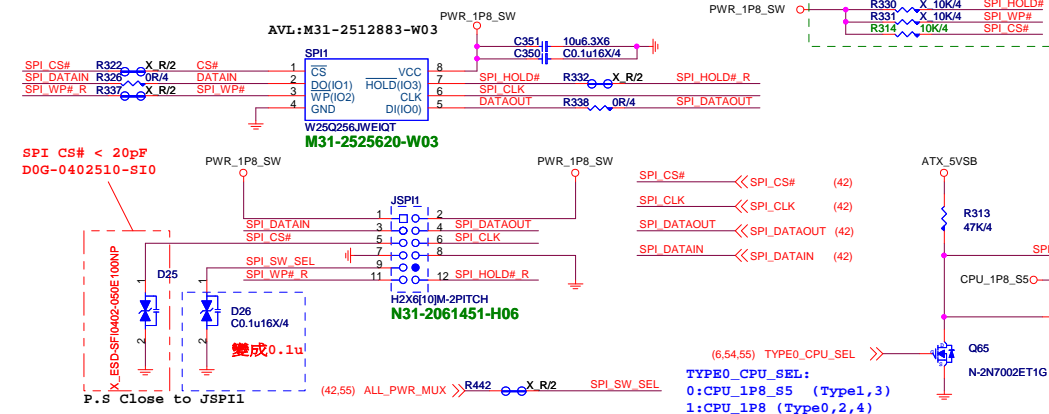
	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode



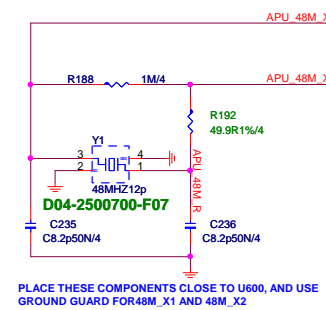
MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size	Document Description	Rev
Custom	AM4 LPC/SPI/USB/CLK/STRAP	1.2
Date:	Monday, April 01, 2019	Sheet 7 of 75



SPI ROM(1.8V)



Layout: Place x'tal within 1.5 inch of APU



GND

AM4
PART 9 OF 9

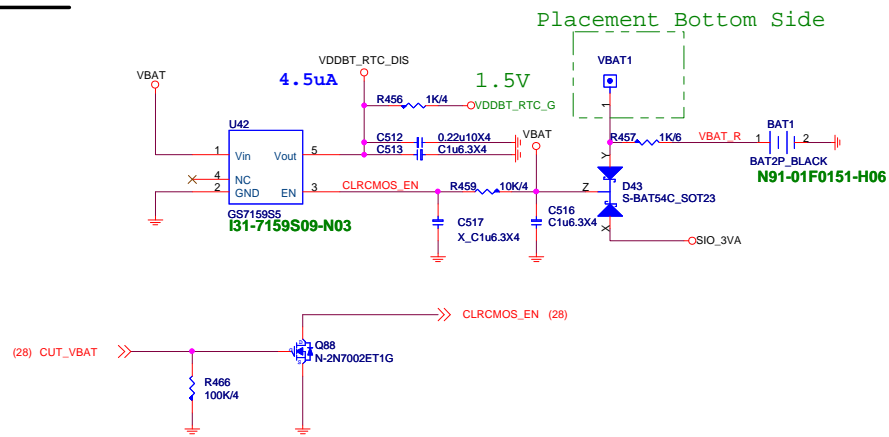


MICRO-STAR INT'L CO.,LTD

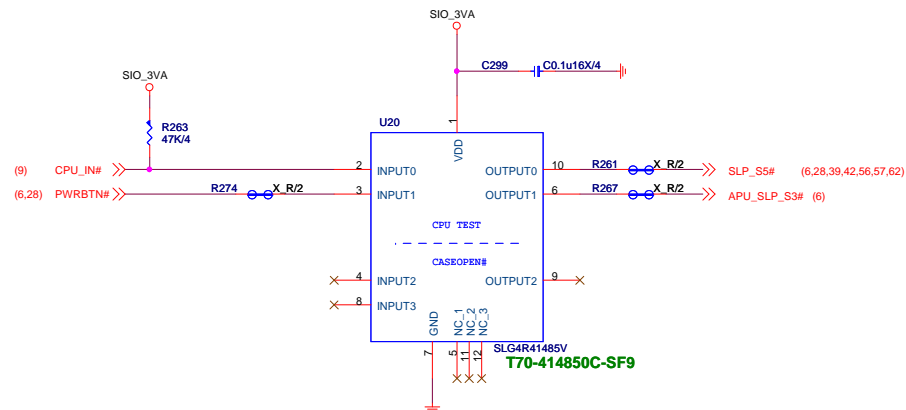
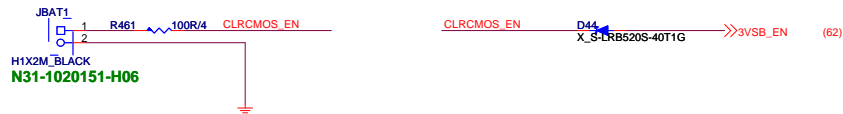
MS-7C37

Size	Document Description	Rev
Custom	AM4 GND	1.2
Date: Monday, April 01, 2019		Sheet 9 of 75

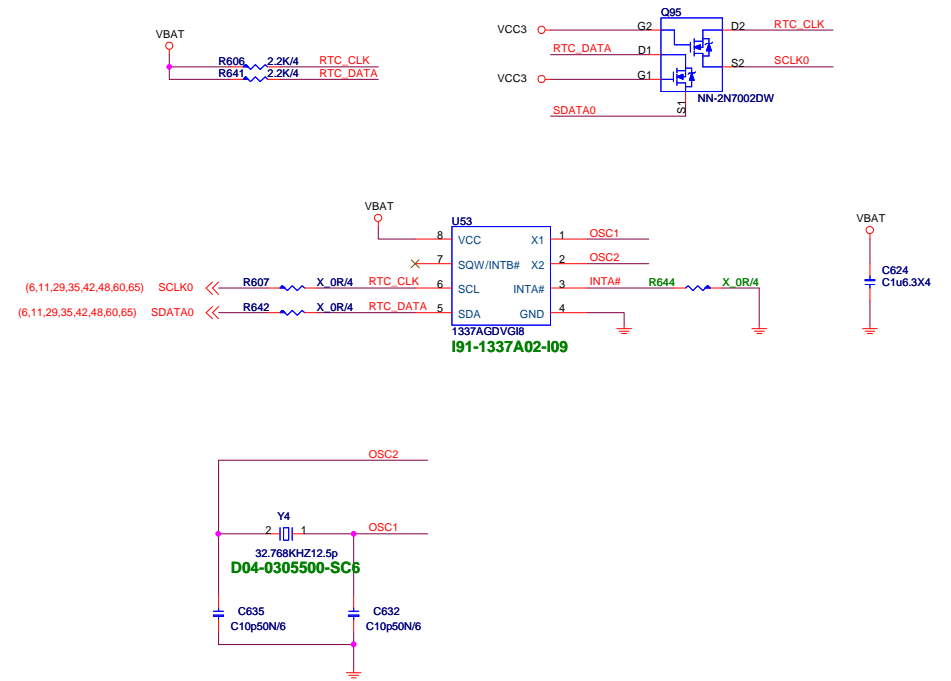
RTC & Clear CMOS Circuit

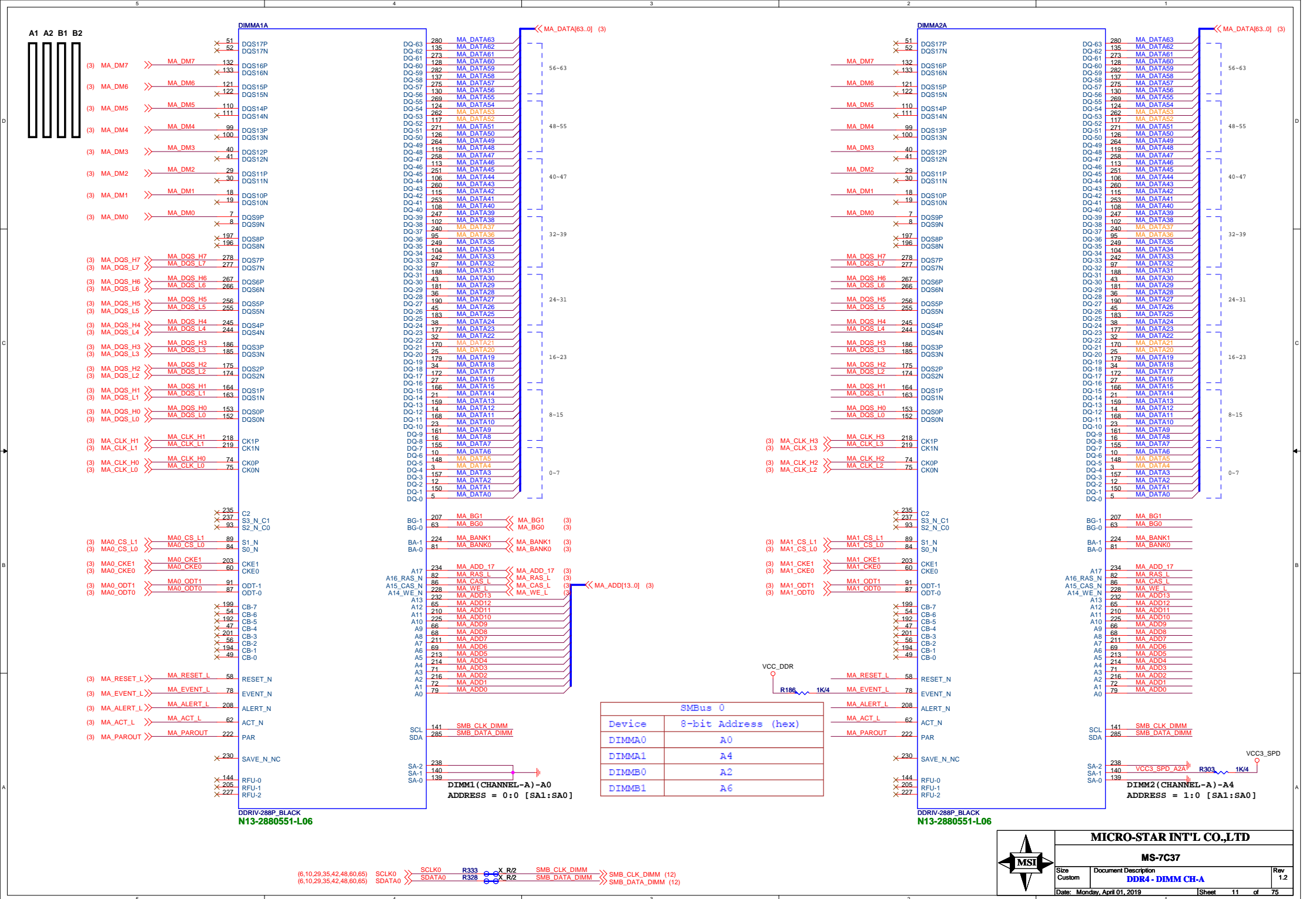


Clear CMOS button



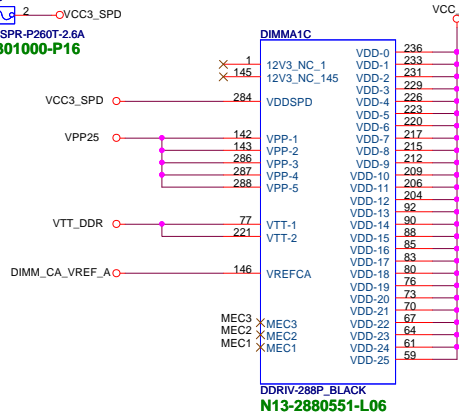
RTC Backup



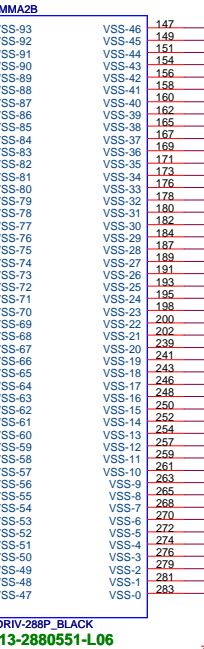
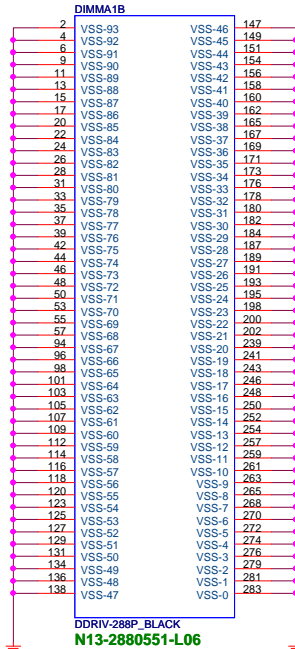
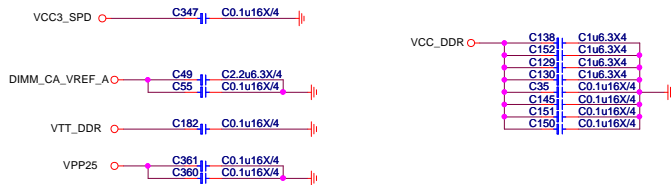


av1:D08-0301100-B07

VCC3 SPD
F5
F-SPR-P260T-2.6A
D08-0301000-P16

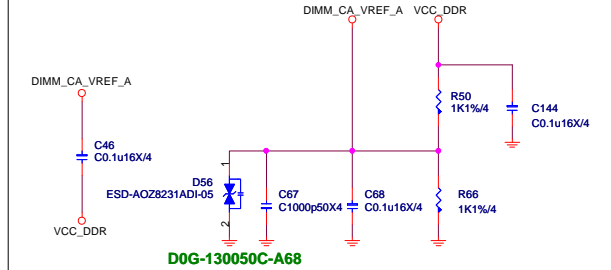


DIMM SLOT PN BY SPEC



DDR VREF

(place resistors close to DIMMs)



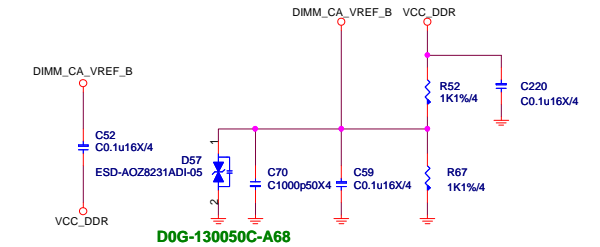
MICRO-STAR INT'L CO.,LTD

MS-7C37

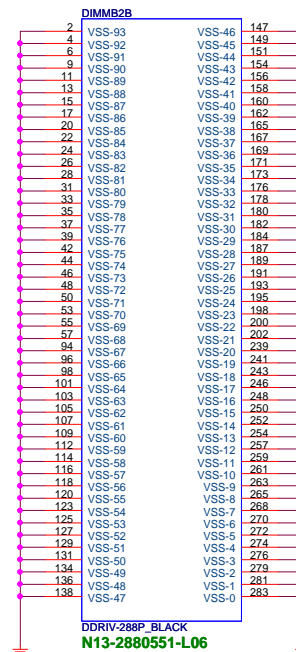
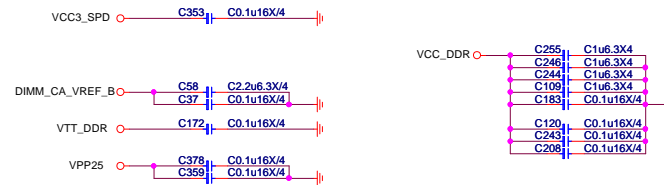
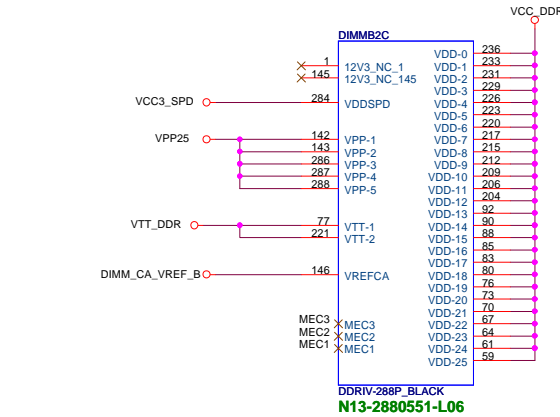
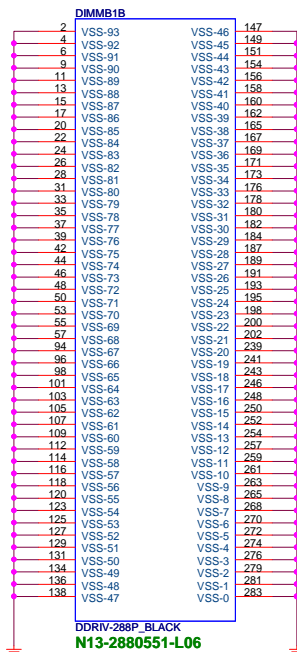
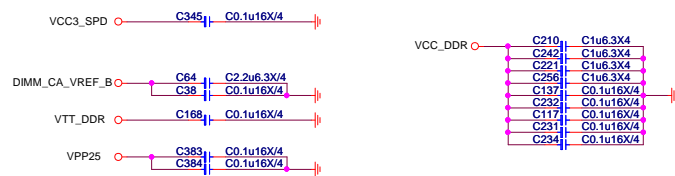
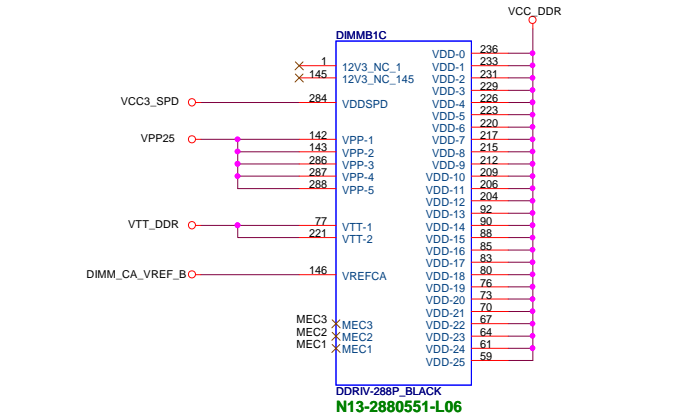
Size	Document Description	Rev
Custom	DDR4 - POWER/GND-1	1.2
Date:	Monday, April 01, 2019	Sheet 13 of 75

DDR VREF

(place resistors close to DIMMs)



D0G-130050C-A68

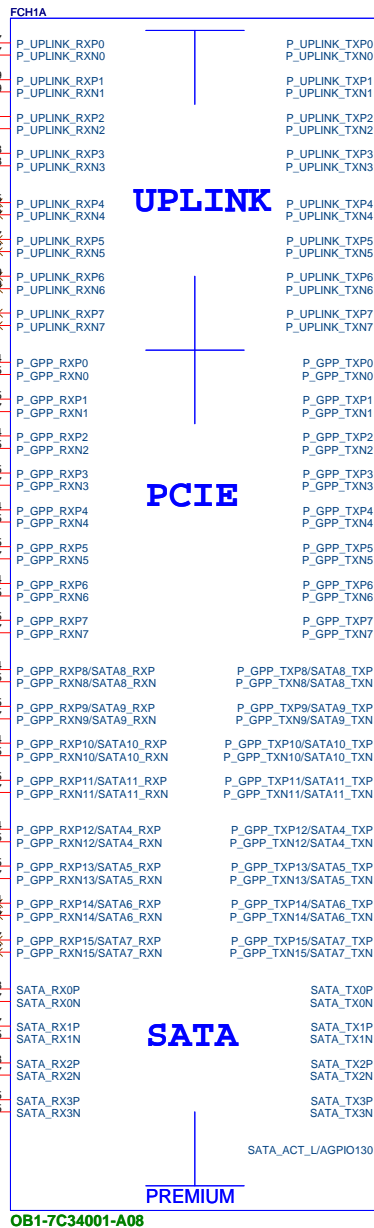
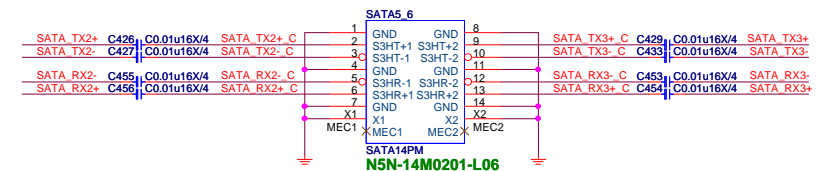
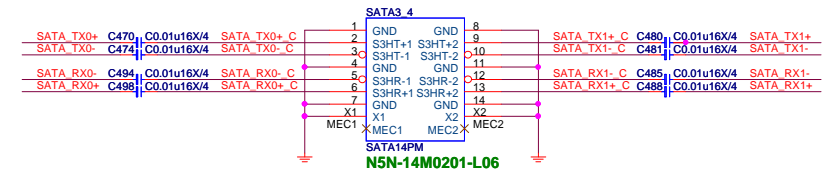


MICRO-STAR INT'L CO.,LTD

MS-7C37

Size	Document Description	Rev
Custom	DDR4 - POWER/GND-2	1.2
Date:	Monday, April 01, 2019	Sheet 14 of 75

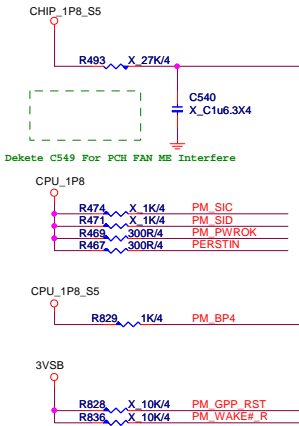
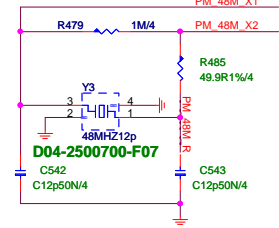
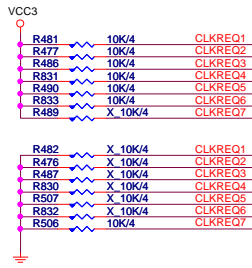
SATA Connector



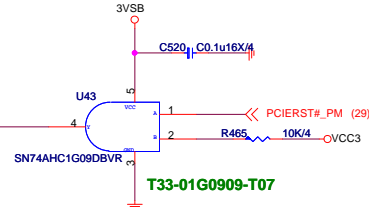
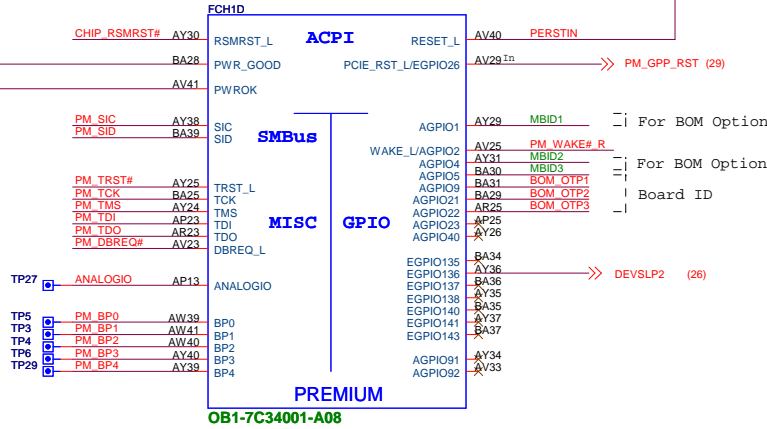
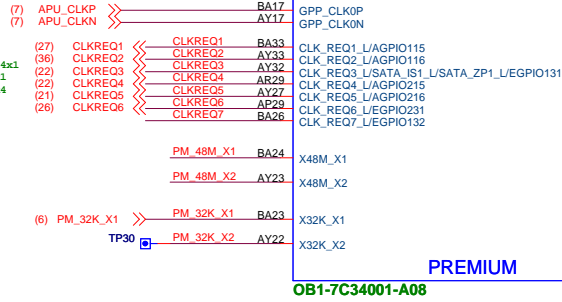
MICRO-STAR INT'L CO.,LTD

MS-7C37

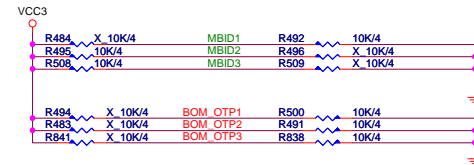
Size	Document Description	Rev
Custom	Premium - PCIE/SATA	1.2
Date:	Monday, April 01, 2019	Sheet 15 of 75



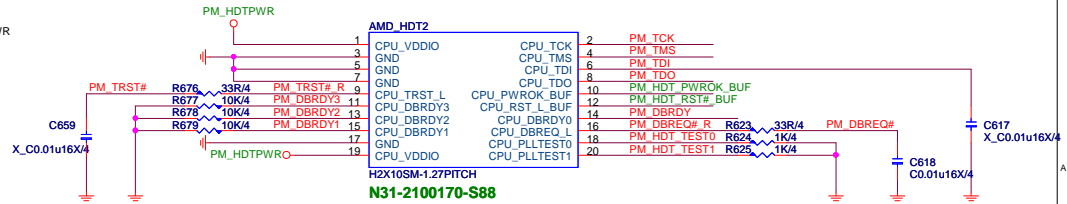
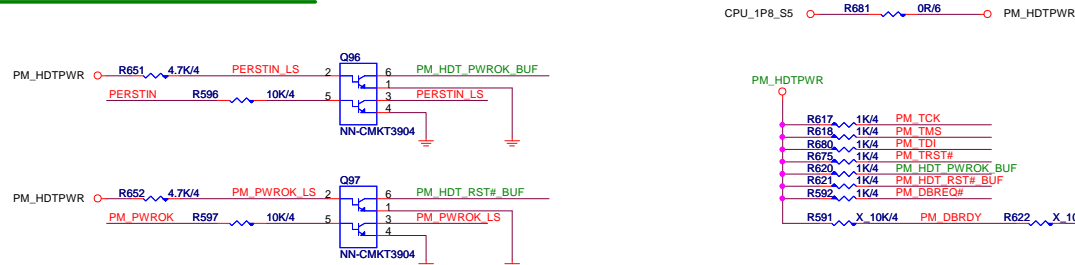
WIFI+BT
LAN
PCIE_E2/4x1
PCIE_E3x4
M.2_2
ASM1061



BOM OPTION



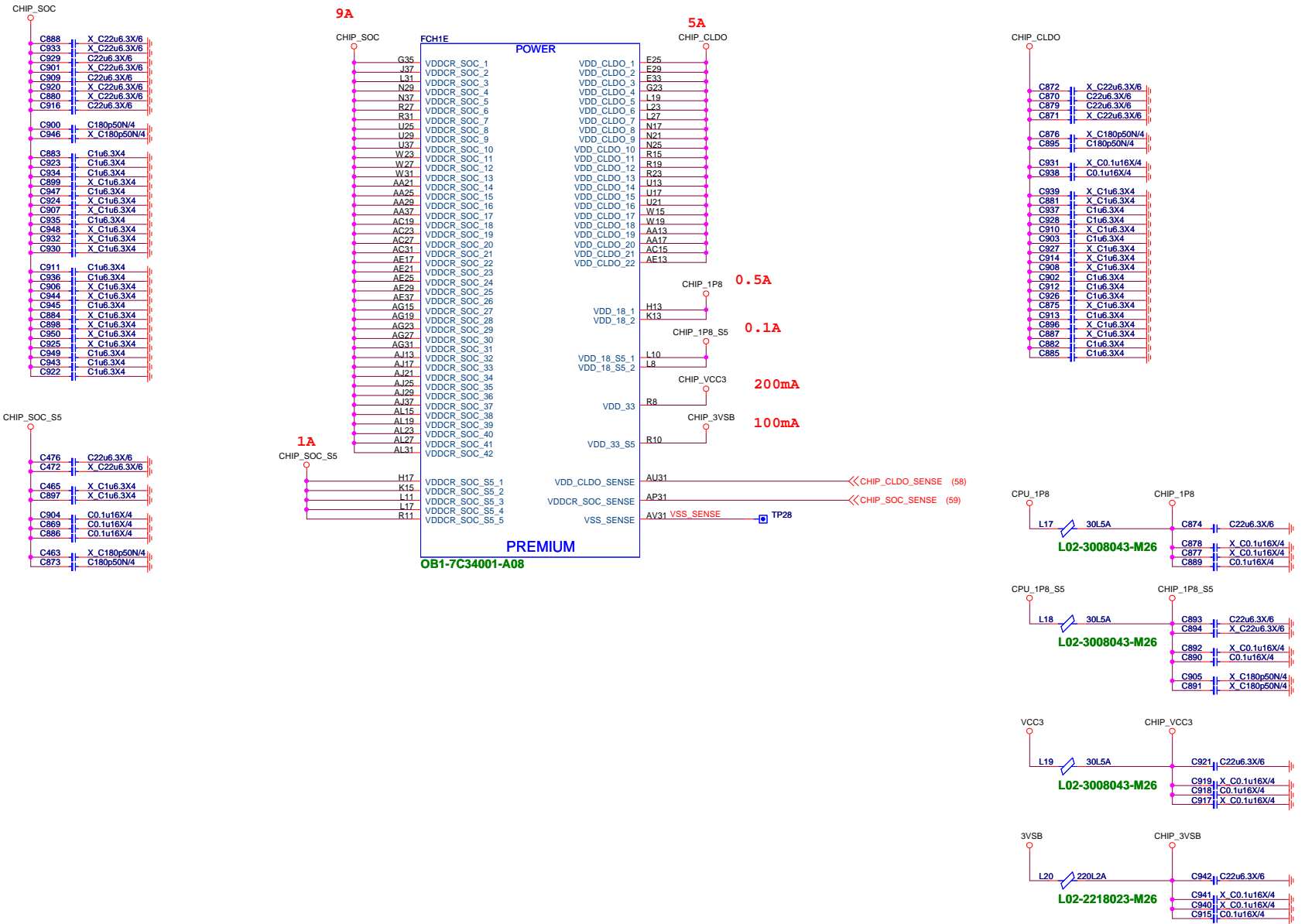
PREMIUM CHIPSET_HDT

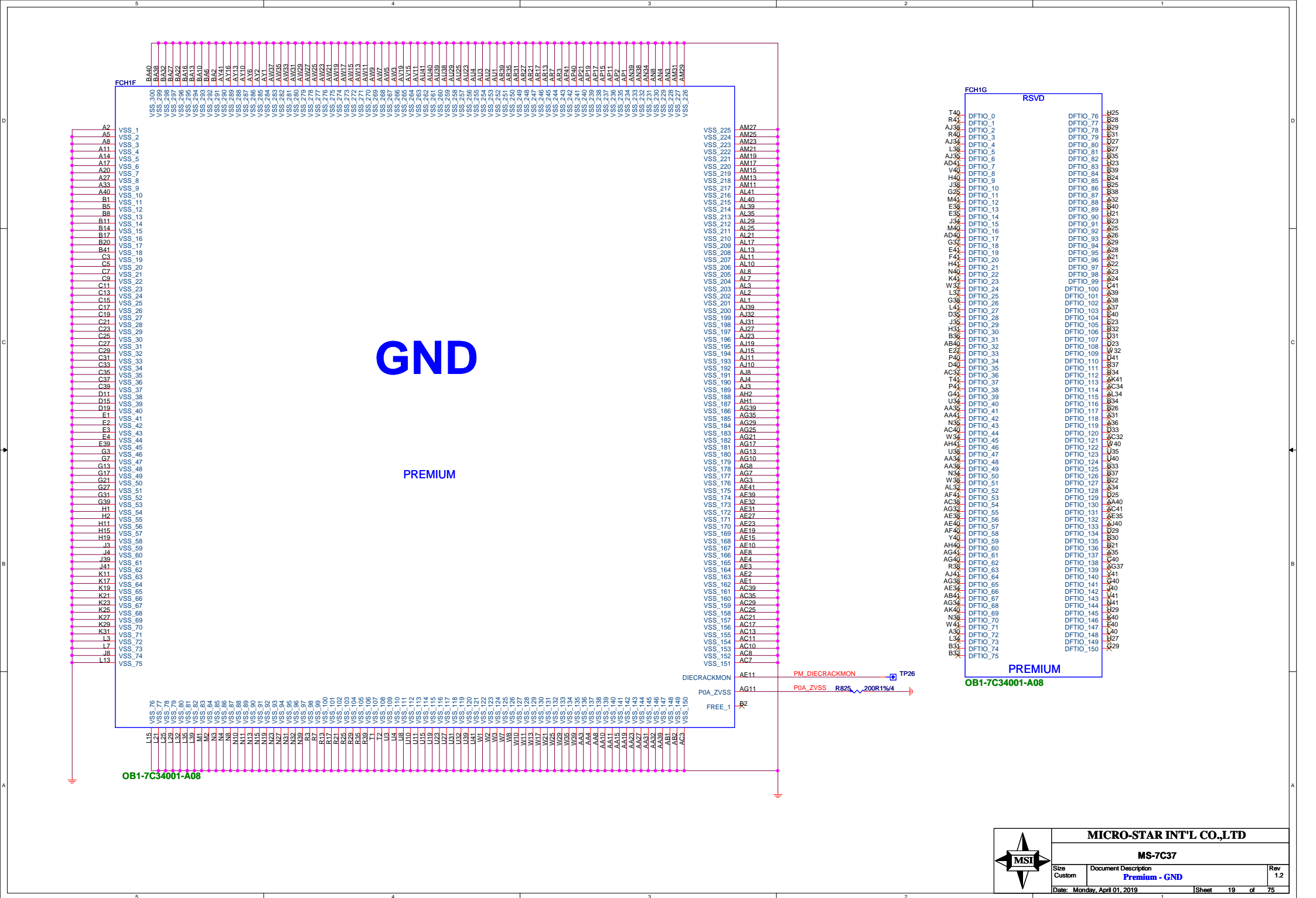


MICRO-STAR INT'L CO.,LTD

MS-7C37

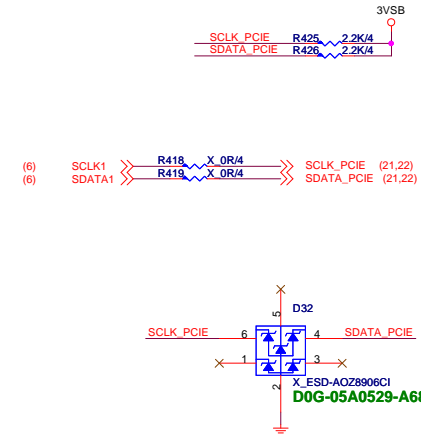
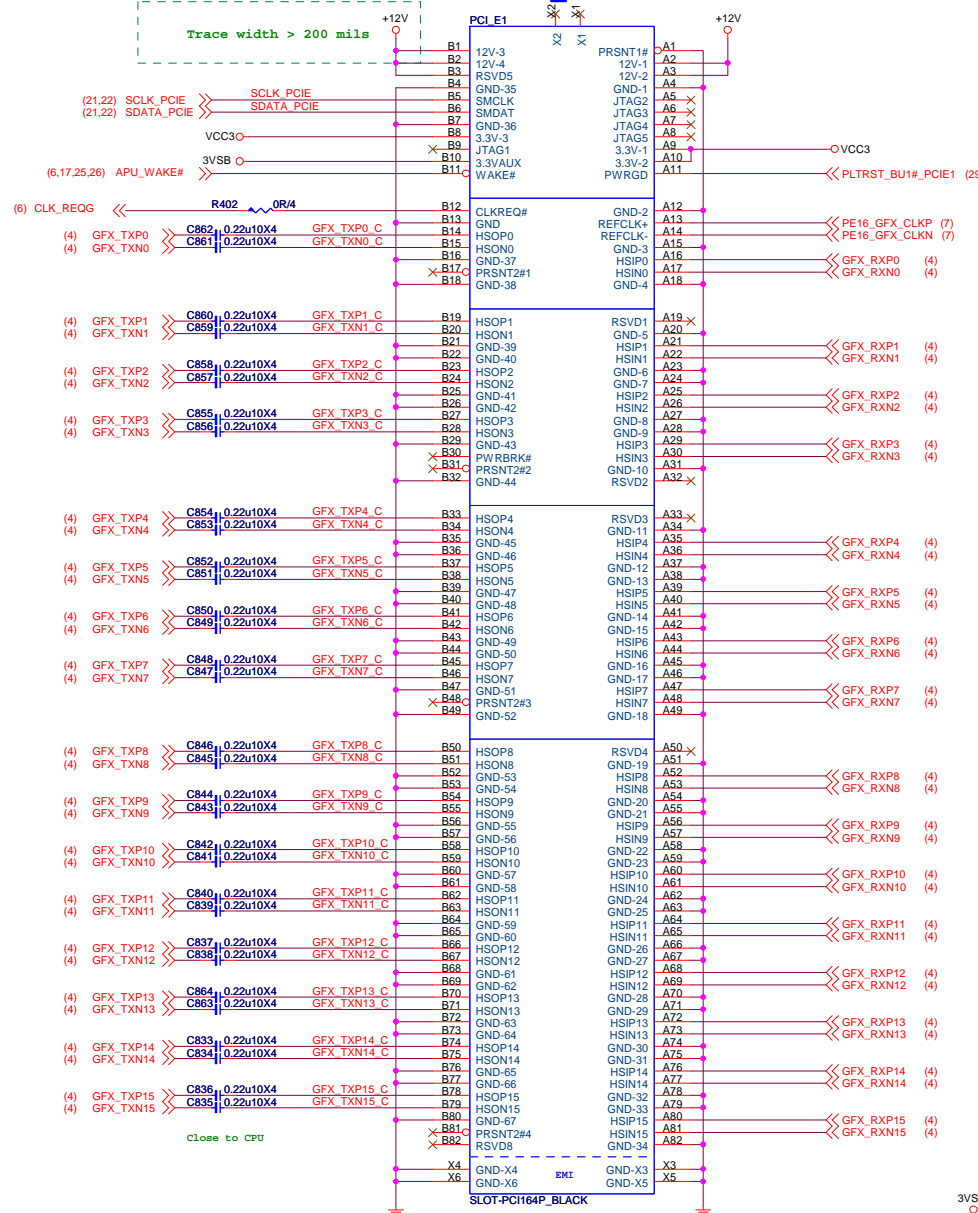
Size	Document Description	Rev
Custom	Premium - CLK/ACPI/GPIO	1.2
Date: Wednesday, April 03, 2019	Sheet 17 of 75	



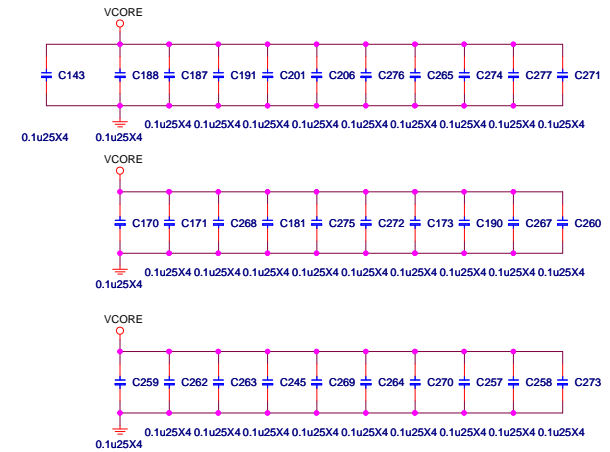


PCI EXPRESS x16 Slot

PCI E1



Bypass Capacitor For Across Moat



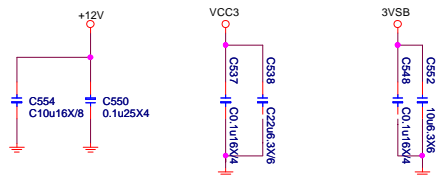
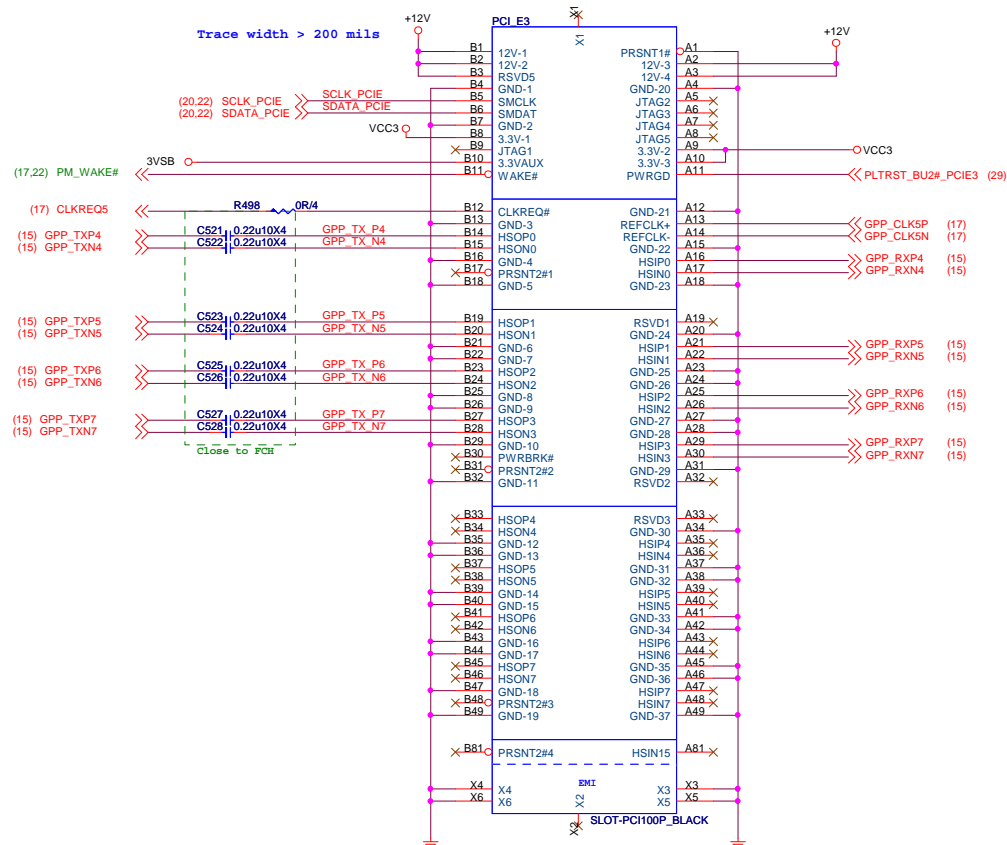
PCI Express x16 Slot

+12V	- 5.5A
+VCC3	- 3A
+3V3_S5 (wake)	- 375mA
+3V3_S5 (no wake)	- 20mA



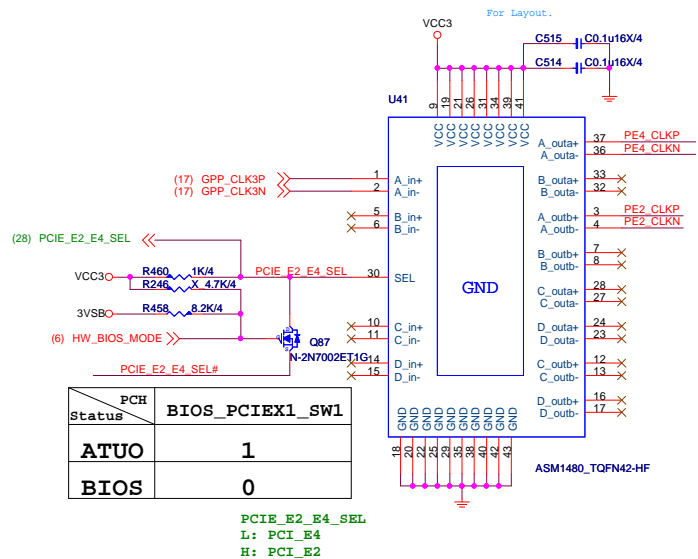
MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size Custom	Document Description	Rev 1.2
PCI E1 (X16)		
Date: Monday, April 01, 2019	Sheet 20	of 75

PCI_E3 X4

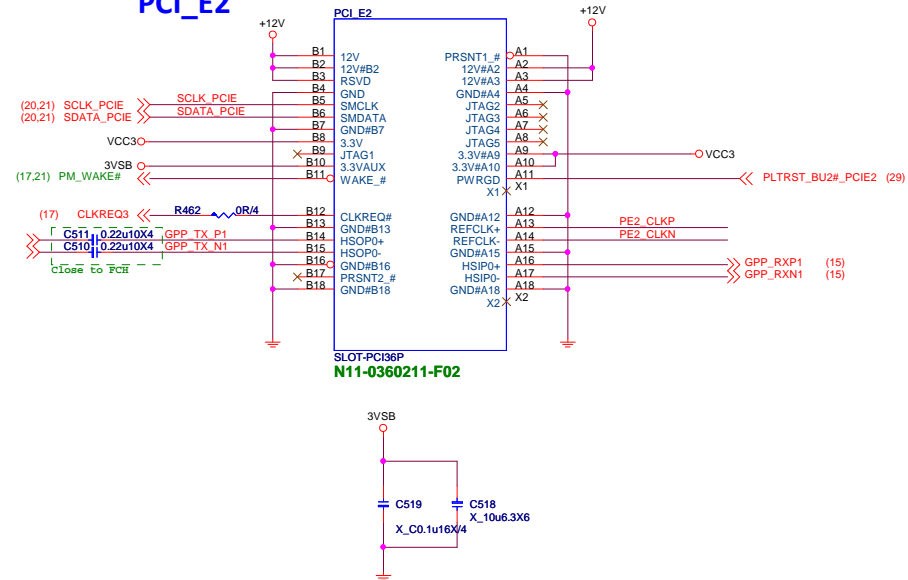


PCI Express x4 Slot *1		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size Custom	Document Description PCI_E3 (X4)	Rev 1.2
Date: Monday, April 01, 2019	Sheet 21 of 75	

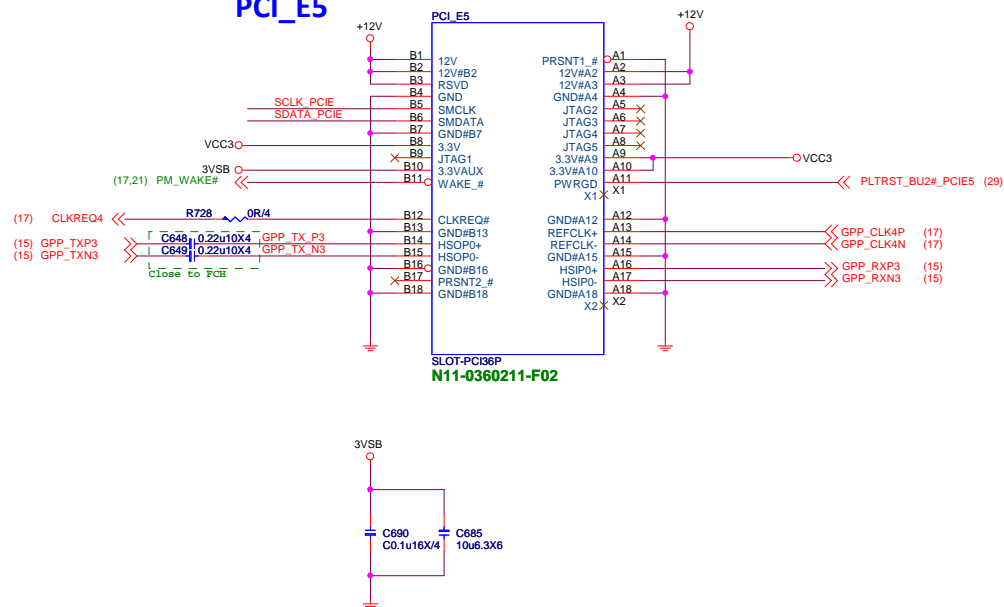


PCI_E2

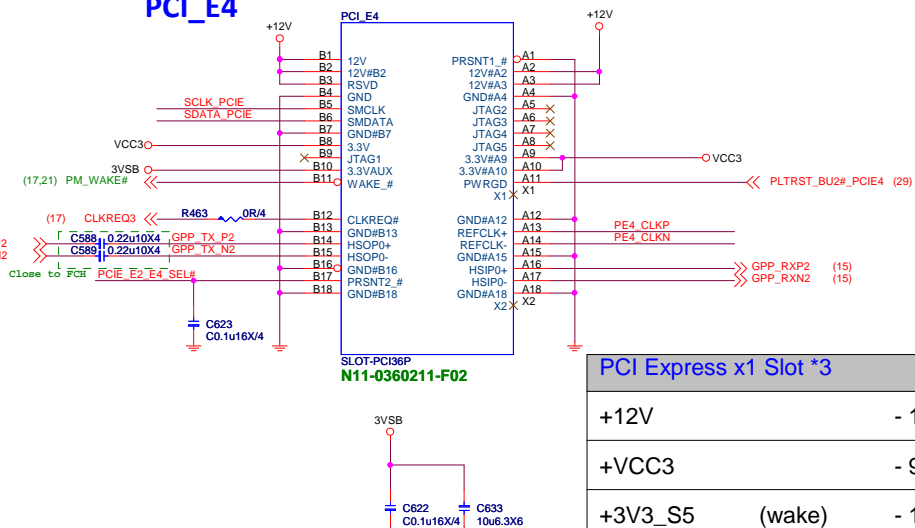


PCIE_E2 & PCIE_E4互切, PCIE_E2 & PCIE_E4同時有PCIE device 以PCIE_E4 優先

PCI_E5



PCI_E4



PCI Express x1 Slot *3

+12V	- 1.5 A
+VCC3	- 9A
+3V3_S5 (wake)	- 1125mA
+3V3_S5 (no wake)	- 60mA



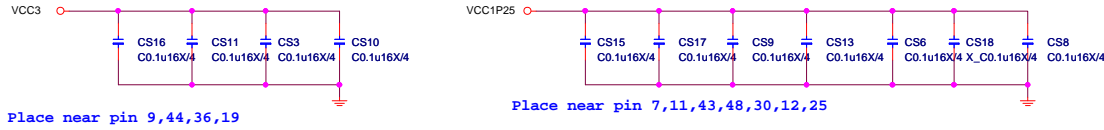
MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size Custom	Document Description	Rev 1.2
PCIE Switch PCI_E2 / E4 / E5 (XI)		
Date: Monday, April 01, 2019	Sheet 22 of 75	

SATA Connector

1.2V delay from 3.3V 90% > 0ms

ASM1061 POWER Consumption

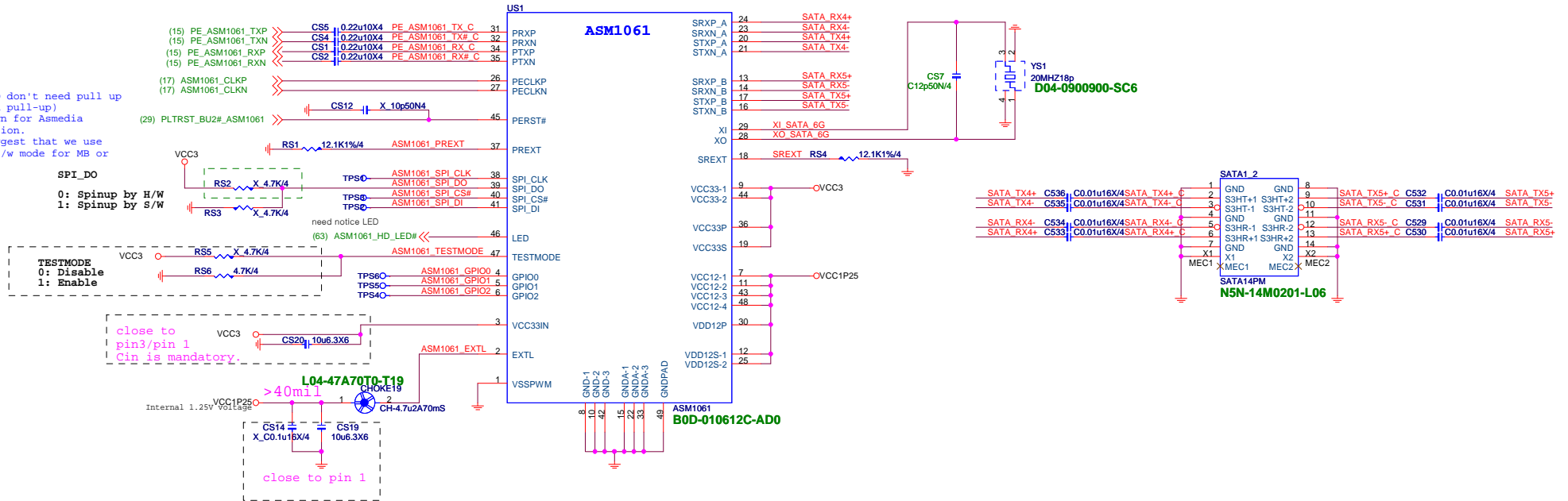
	3.3V	1.25V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47

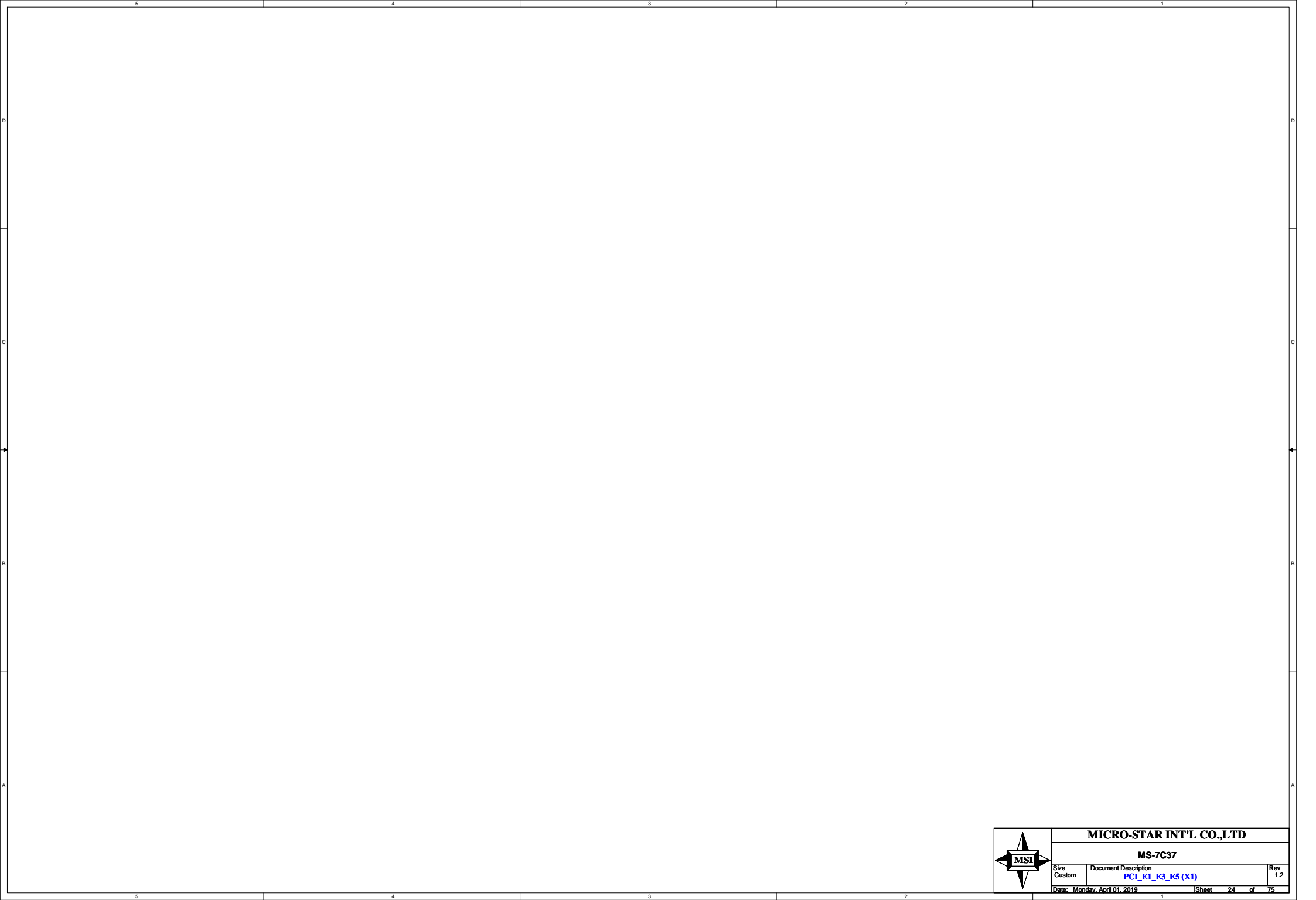


ASM1061 SATA6G

SATA_SPI_DO don't need pull up (integrated pull-up) or pull down for Asmedia recommendation.
Asmedia suggest that we use spinup by s/w mode for MB or PCI-E Card.

SPI_DO
0: Spinup by H/W
1: Spinup by S/W





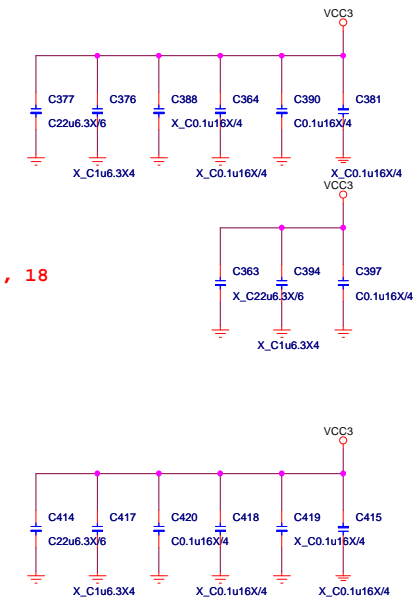
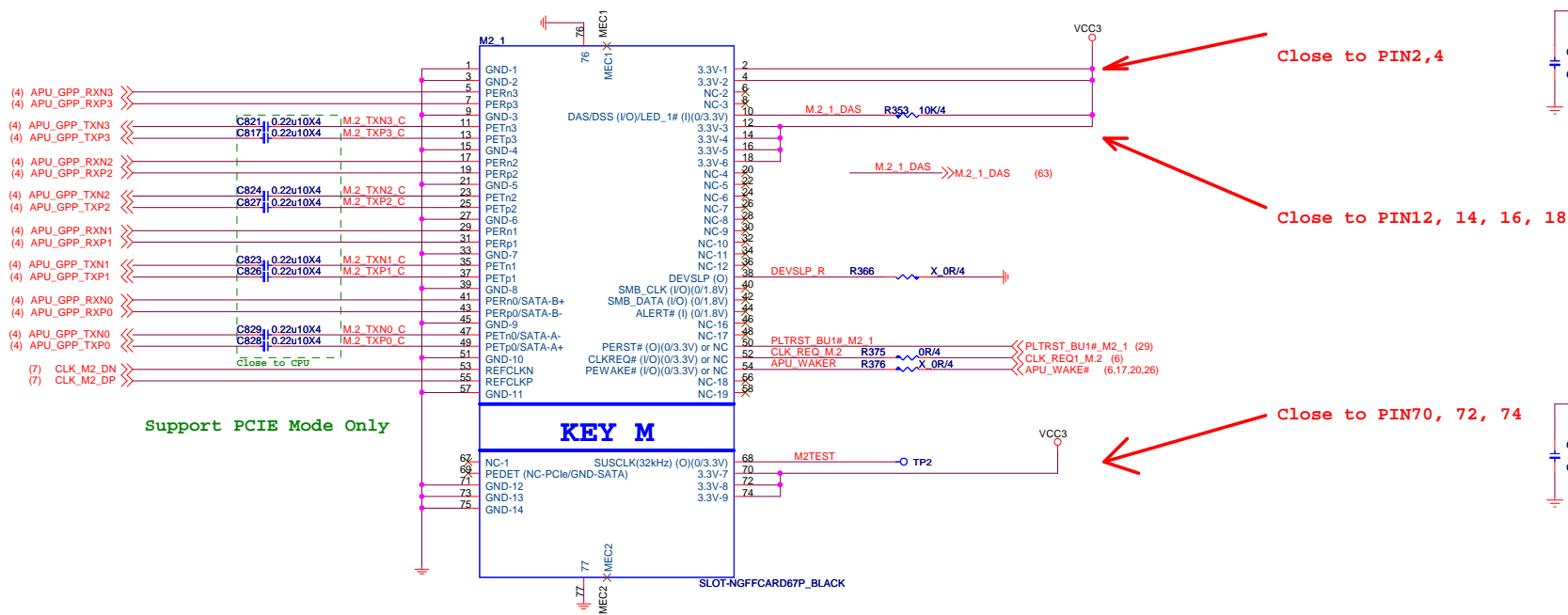
MICRO-STAR INT'L CO.,LTD

MS-7C37

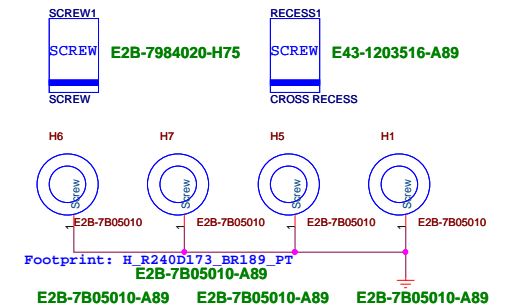
Size Custom	Document Description PCI_E1_E3_E5 (X1)	Rev 1.2
Date: Monday, April 01, 2019		
Sheet 24 of 75		

M.2 1 Connector

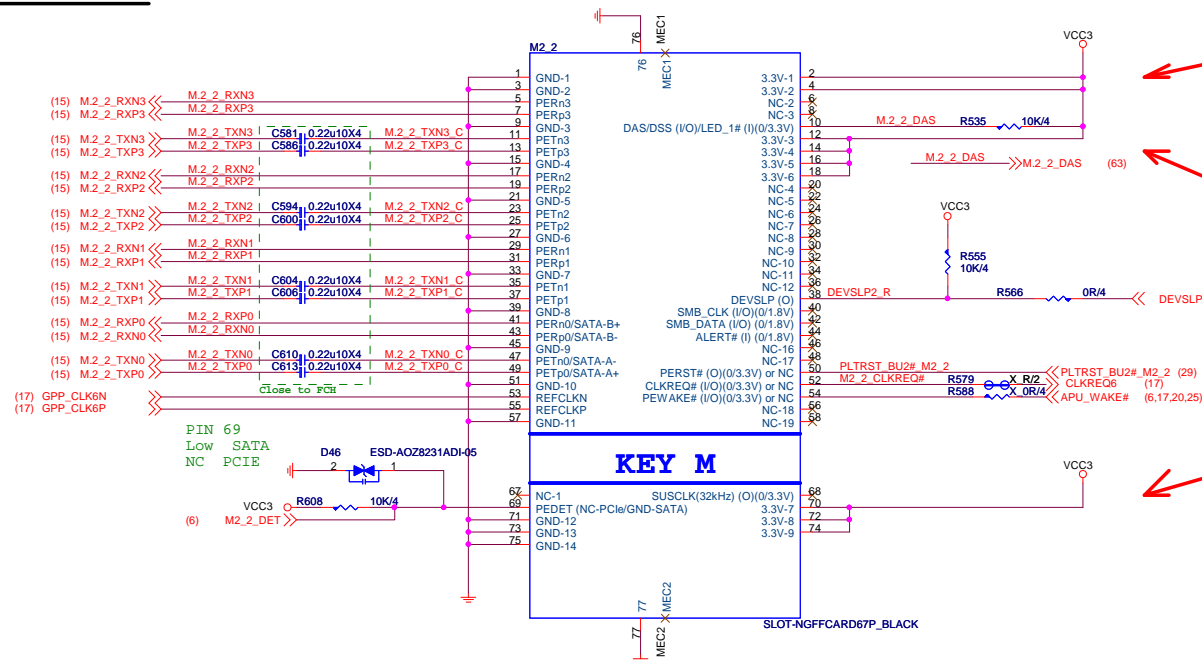
VCC3 4.25A
Max: 14W



22 * 110

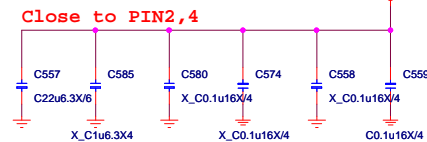


M.2_2 Connector

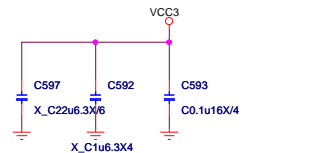


Support PCIE and SATA Mode

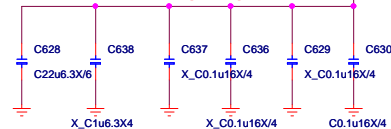
VCC3 4.25A
Max: 14W



Close to PIN12, 14, 16, 18



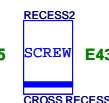
Close to PIN70, 72, 74



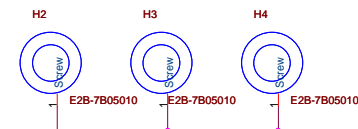
22 * 80



E2B-7984020-H75



E43-1203516-A89



Footprint: H_R240D173_BR189_PT

E2B-7B05010-A89 E2B-7B05010-A89
E2B-7B05010-A89



MICRO-STAR INT'L CO.,LTD

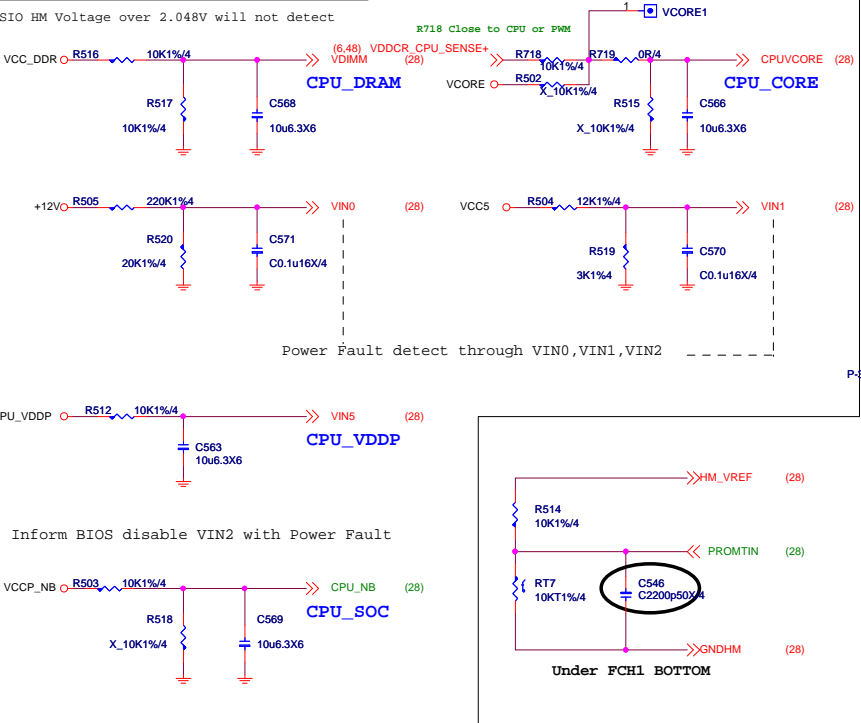
MS-7C37

Size Custom	Document Description M2_2	Rev 1.2
Date: Monday, April 01, 2019		Sheet 26 of 75

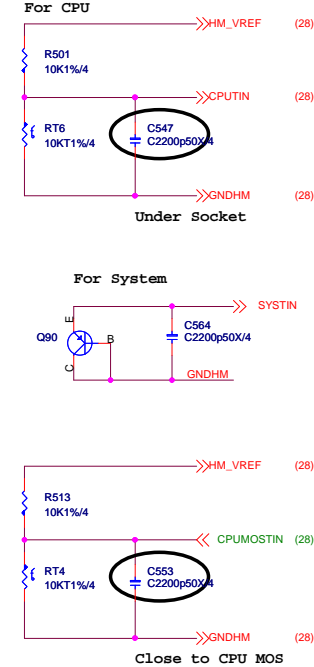
Size Custom	Document Description M2_WIFI+BT	Rev 1.2
Date: Monday, April 01, 2019		Sheet 27 of 75

HW Monitor - Voltage

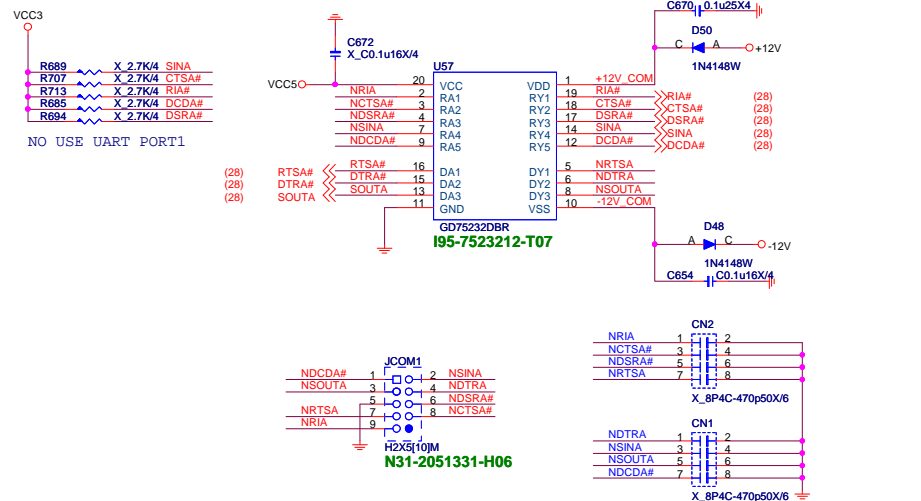
SIO HM Voltage over 2.048V will not detect



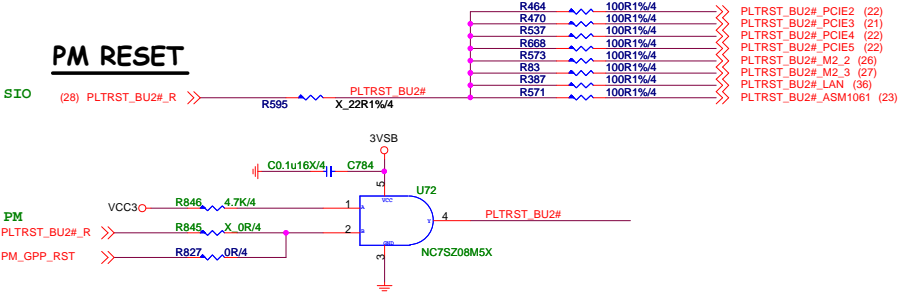
TEMP SENSOR



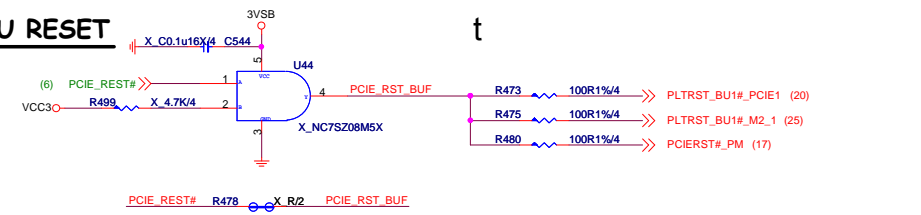
COM PORT



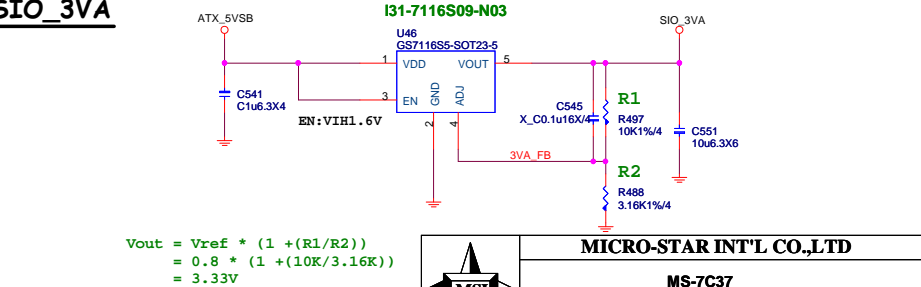
PM RESET



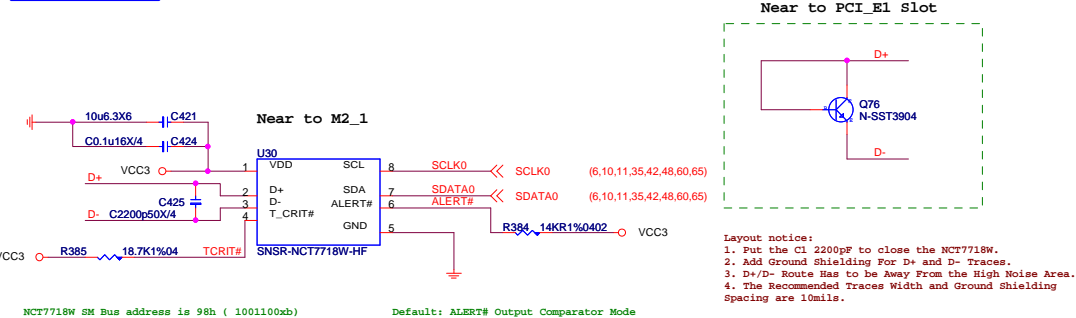
CPU RESET



SIO_3VA



NCT7718W



TEMPERATURE (°C)	T_CRIT#					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

MICRO-STAR INT'L CO.,LTD

MS-7C37

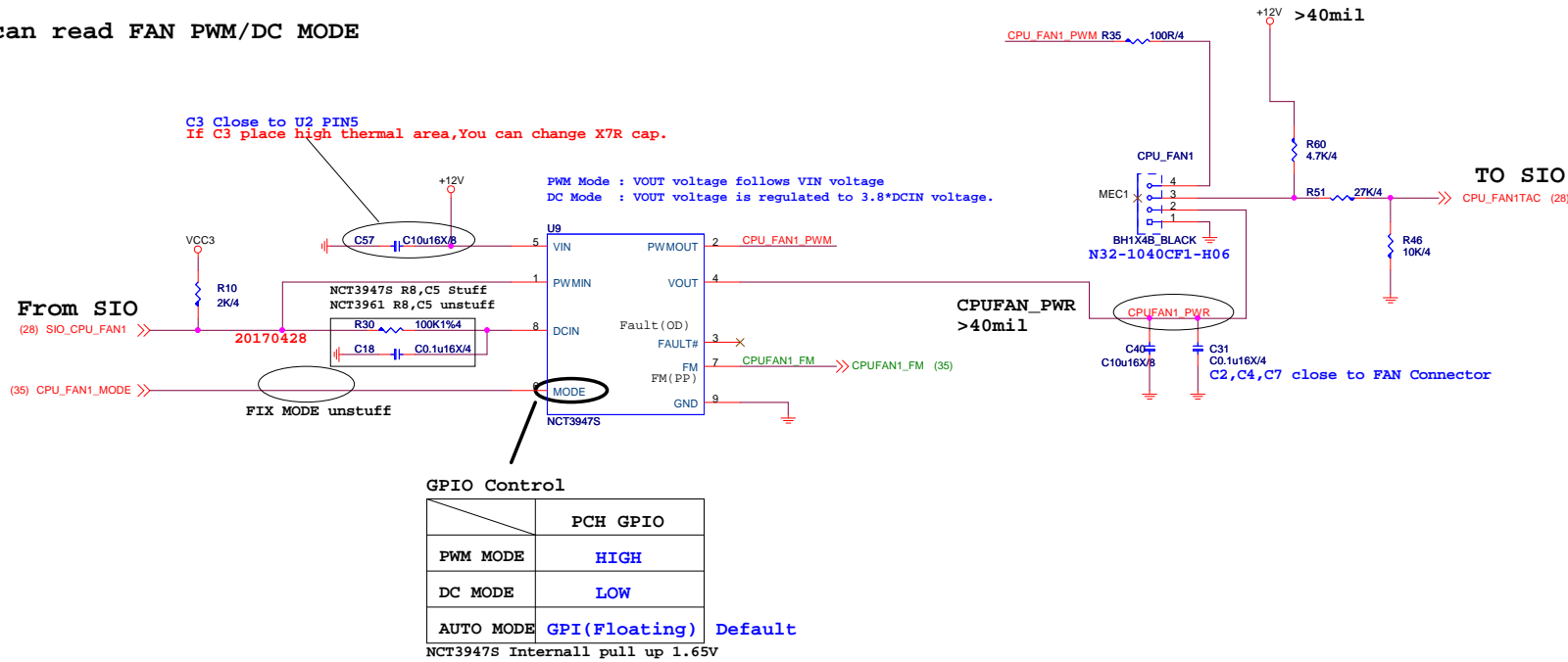
Size	Document Description	Rev
Custom	SIO - HW Monitor / NCT7718W	1.2

Date: Monday, April 01, 2019 | Sheet 29 of 75

TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

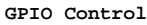
CPUFAN1

- 1.Mode GPIO BIOS can swtich PWM/DC MODE
- 2.FM:BIOS can read FAN PWM/DC MODE



PUMPFAN1

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO	
PWM MODE	HIGH	
DC MODE	LOW	
AUTO MODE	GPI(Floating)	Default

NCT3947S Internall pull up 1.65V



MICRO-STAR INT'L CO.,LTD

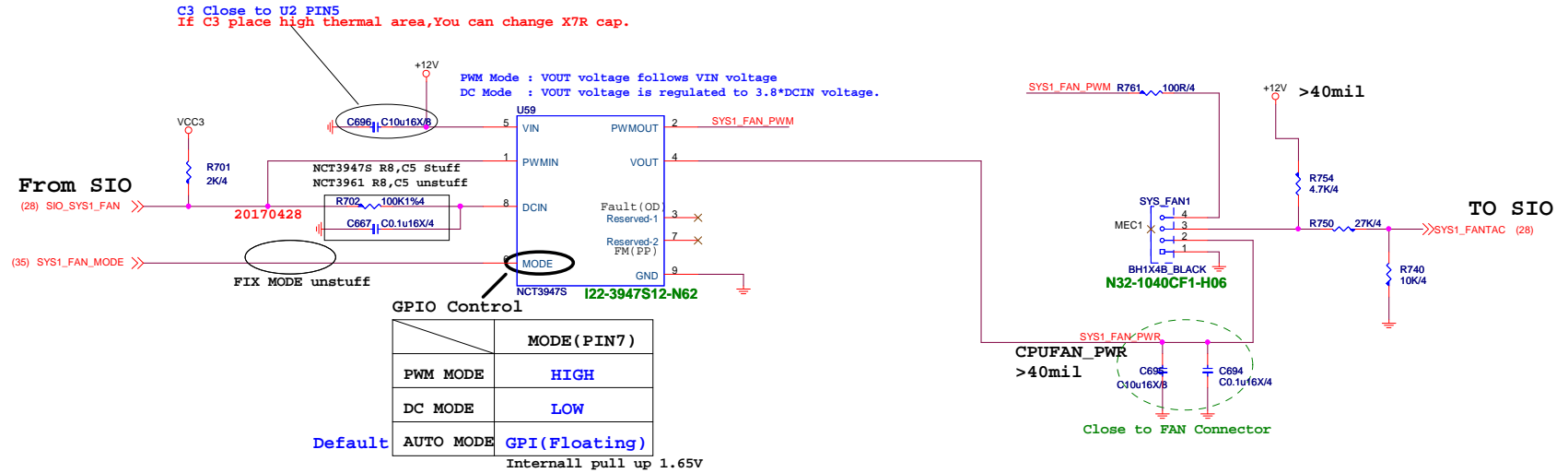
MS-7C37

Size Custom	Document Description FAN TYPE-K PUMPFANI	Rev 1.2
Date: Monday, April 01, 2019	Sheet 31 of 75	

SYSFAN1

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

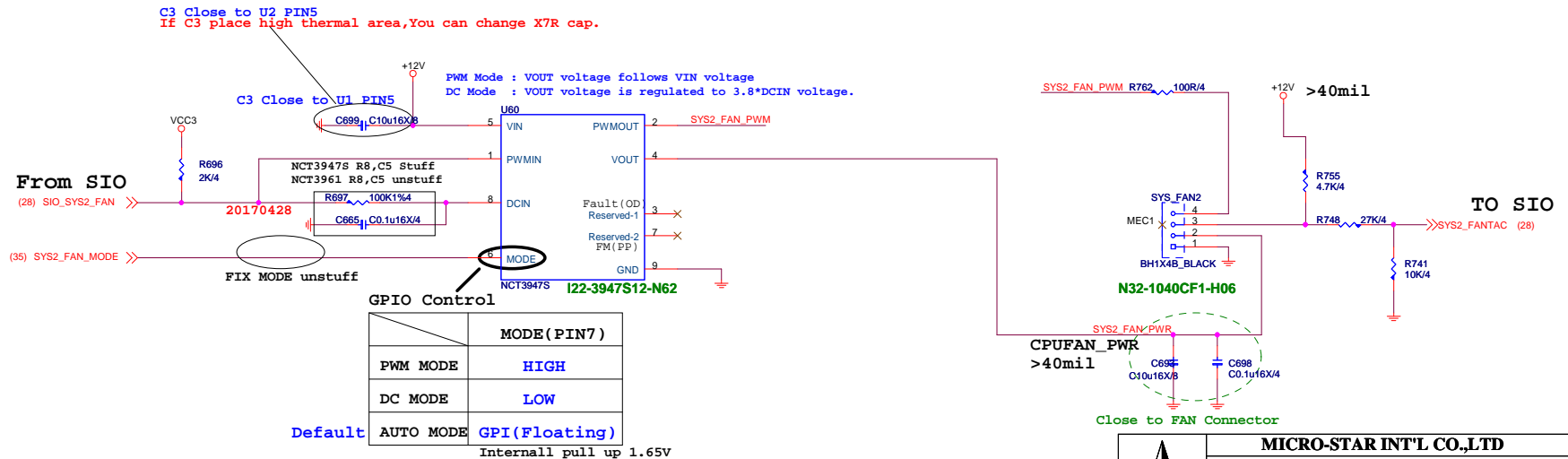
1.Mode GPIO BIOS can switch PWM/DC MODE



SYSFAN2

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE



MICRO-STAR INT'L CO.,LTD

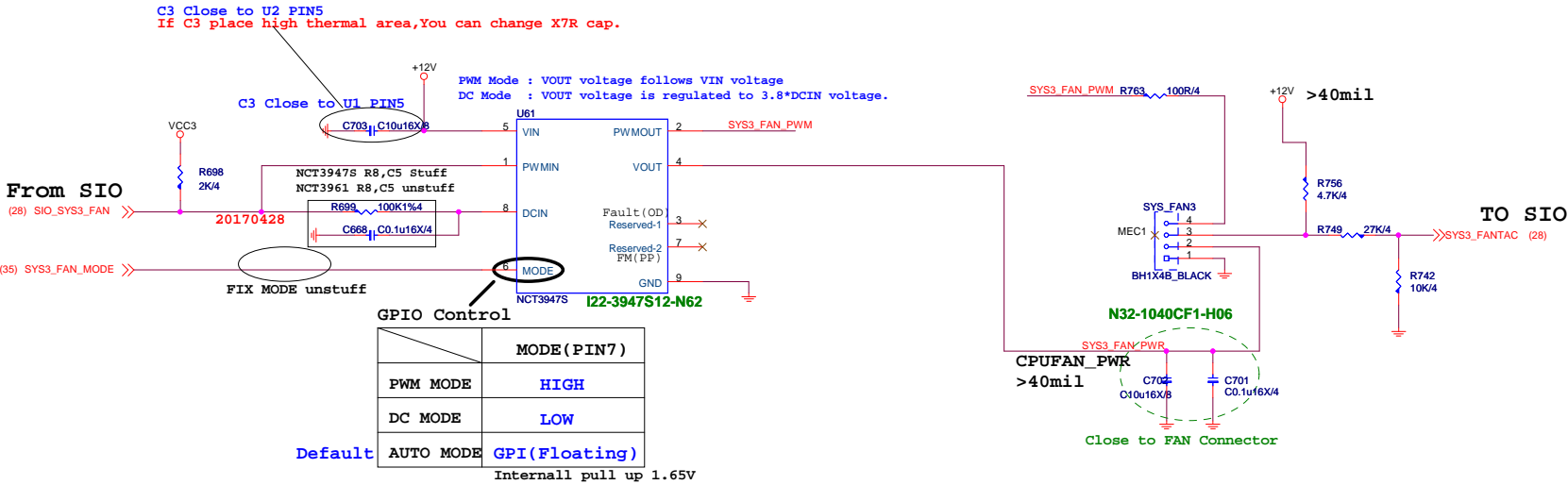
MS-7C37

Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN1/2	1.2
Date:	Monday, April 01, 2019	Sheet 32 of 75

SYSFAN3

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

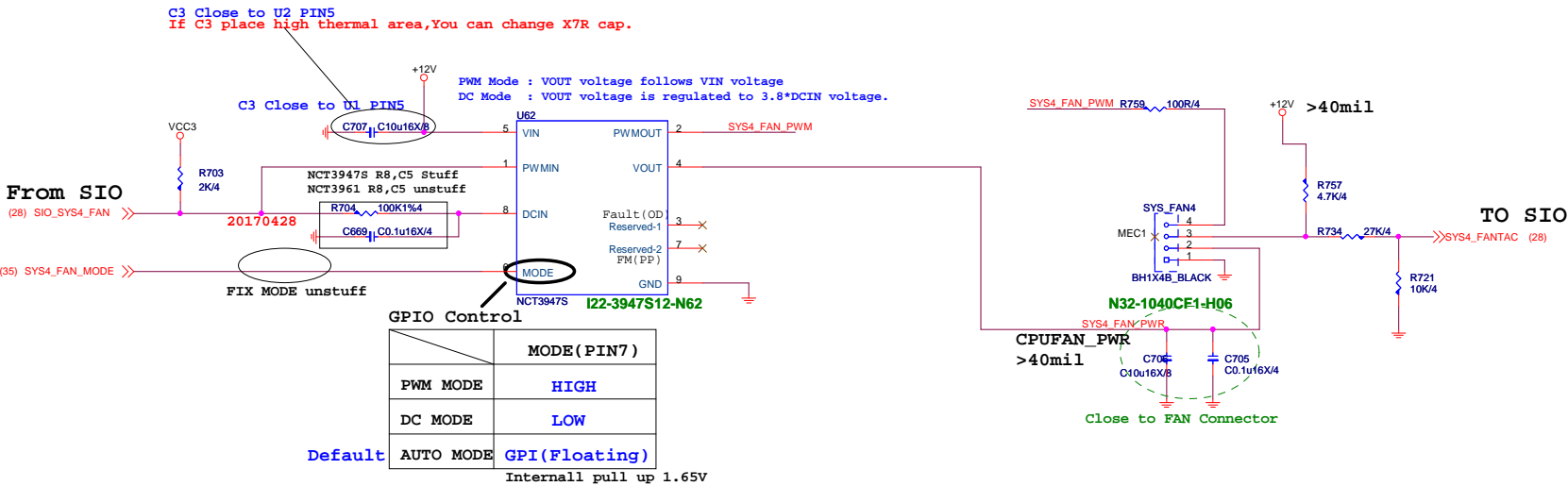
1.Mode GPIO BIOS can switich PWM/DC MODE



SYSFAN4

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switich PWM/DC MODE

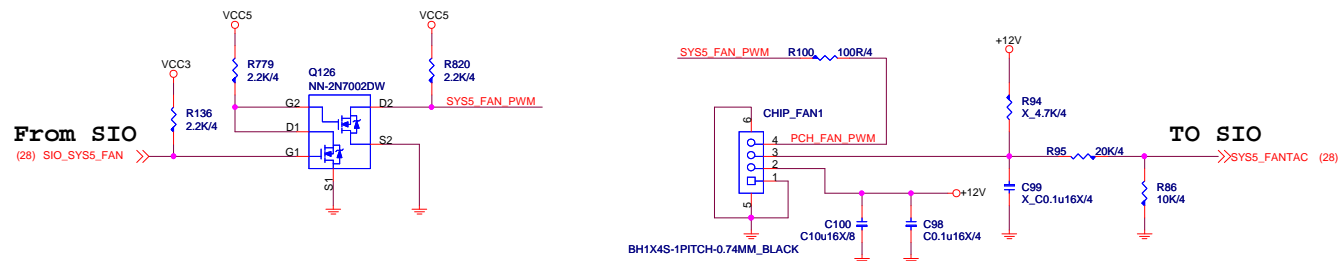


MICRO-STAR INT'L CO.,LTD

MS-7C37

Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN3/4	1.2
Date: Monday, April 01, 2019/		
Sheet 33 of 75		

PCH_FAN



By PM Define FAN name

SHOW FAN FAULT USE	FAN
GP10	CPUFAN1
GP11	CPUFAN2 PUMPFAN

BIOS SHOW FAN FAULT Information USE
Default GPI

BIOS SHOW FAN MODE Information USE
Default GPI

use avoid S5 leakage

CPUFAN1_FM R47 1K/4

By PM Define FAN name

SHOW FAN MODE USE	FAN
GP12	CPUFAN1
GP13	CPUFAN2 PUMPFAN

By PM Define FAN name

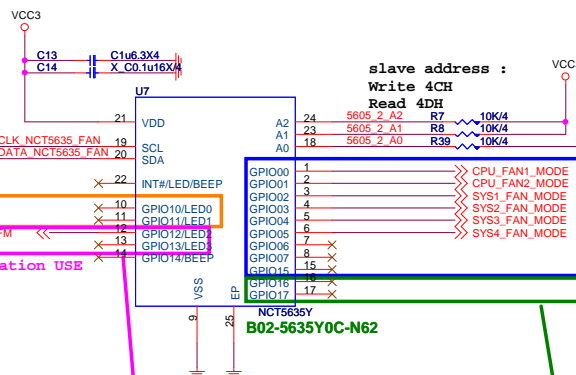
LED OFF BLINK	FAN
GP16	CPUFAN1
GP17	CPUFAN2 PUMPFAN

Default GPI

USE LED OFF & LED BLINK

By PM Define FAN name

FAN MODE USE	FAN
GP00	CPUFAN1
GP01	CPUFAN2 PUMPFAN
GP02	SYSFAN1
GP03	SYSFAN2
GP04	SYSFAN3
GP05	SYSFAN4
GP06	SYSFAN5
GP07	EXT_SYS FAN1
GP15	EXT_SYS FAN2

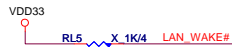


MICRO-STAR INT'L CO.,LTD

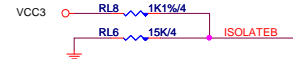
MS-7C37

Size Custom	Document Description FAN GPIO NCT5635	Rev 1.2
Date: Monday, April 01, 2019	Sheet 35 of 75	

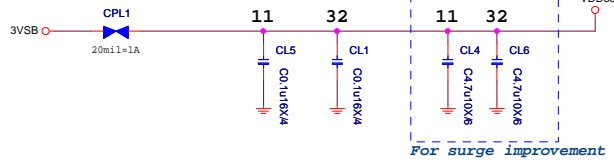
RTL8111H Giga LAN



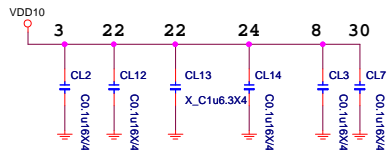
Remove pull-up R if R existence on motherboard
(or SB has internal pull-up R).



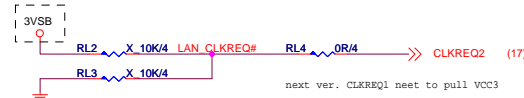
VDD33@65mA



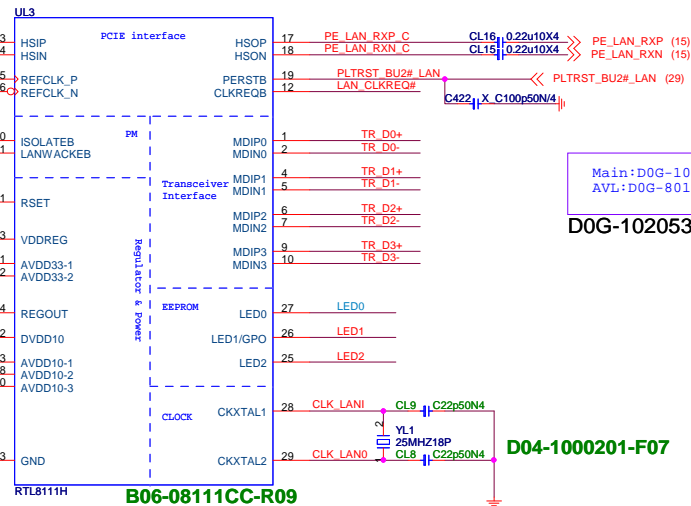
VDD10@150mA



Pull-up resistor RL9 required to either 3.3V suspend or core rail depending on the power well of the PCH input CLKREQ# buffer.

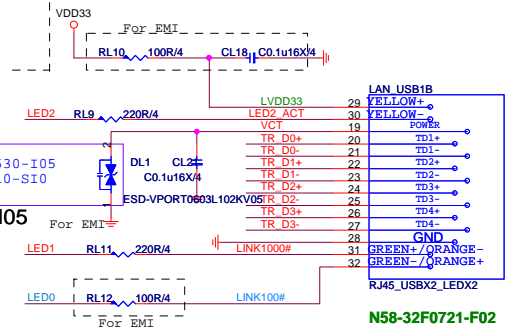


Pin33: 4 via from top layer to GND layer and make the via at the center of IC.

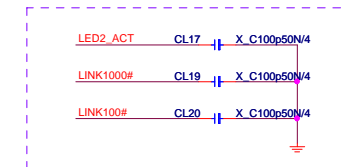


```
| PIN19:  
| AMD platform connect to PCIE_RST#,  
| don't connect to A-RST#.  
| INTEL platform connect to PLT_RST#,
```

LAN Connector



For EMI

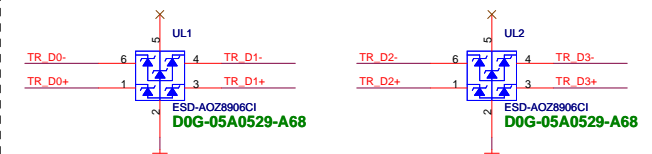


8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

ESD Protect
close to connector

D0G-0200529-A68
D0G-0100619-I05

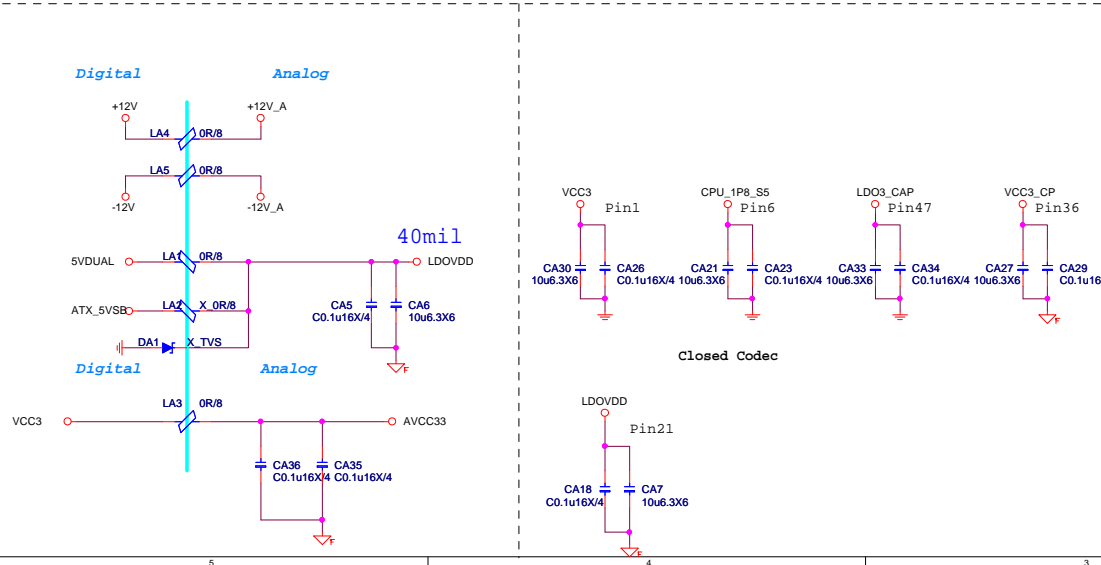
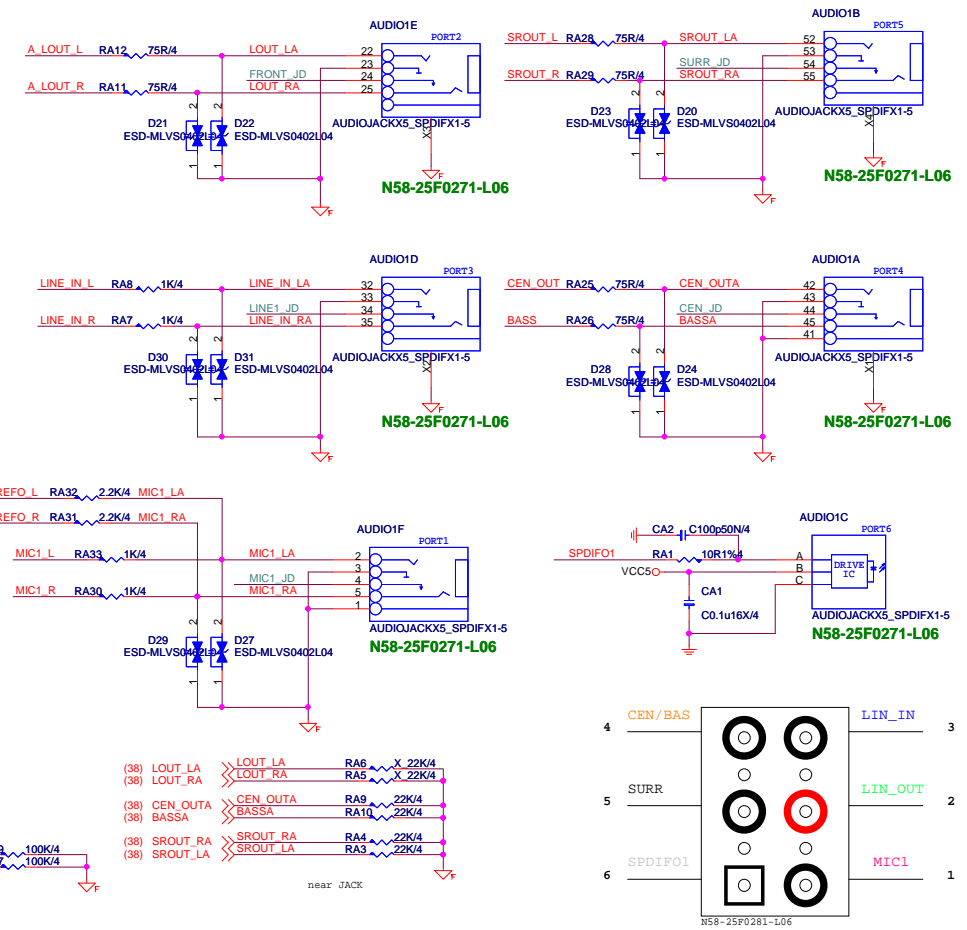
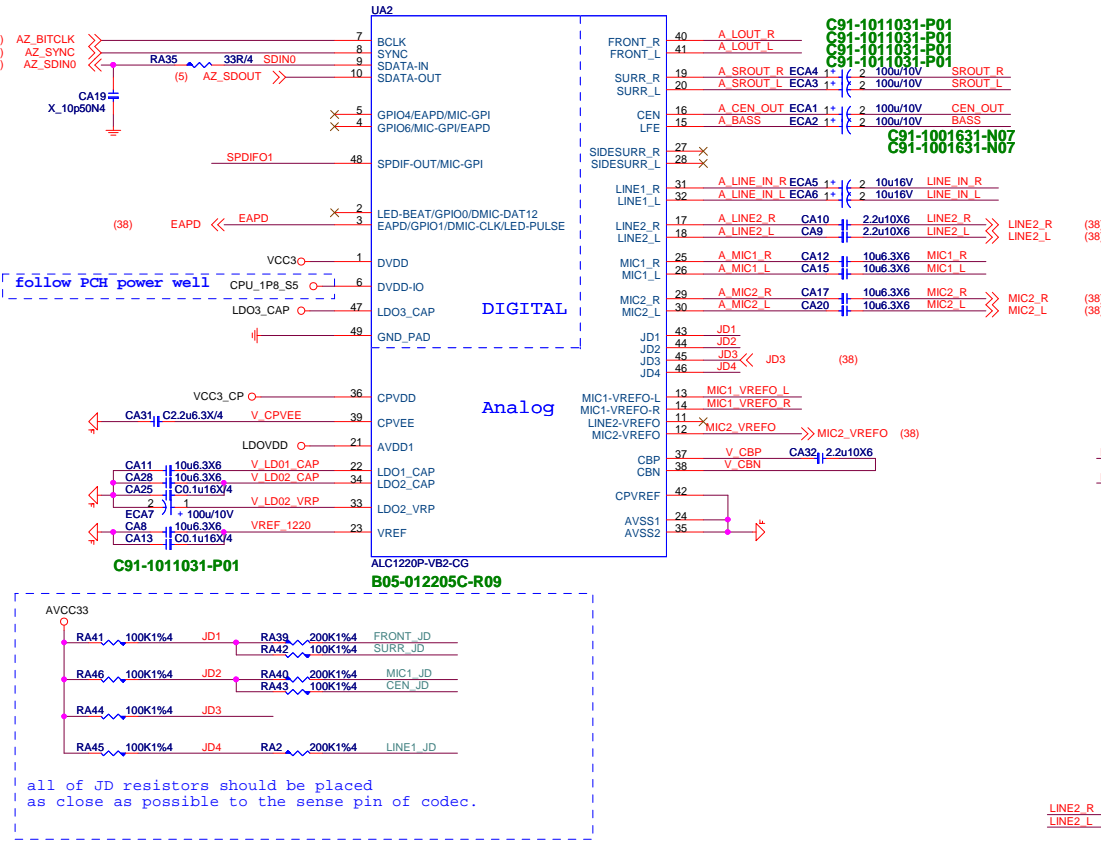


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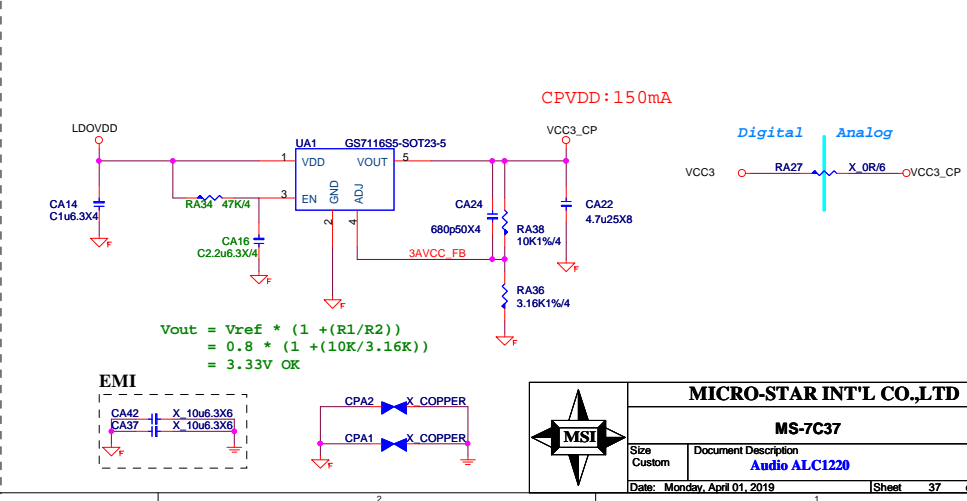
MS-7C37

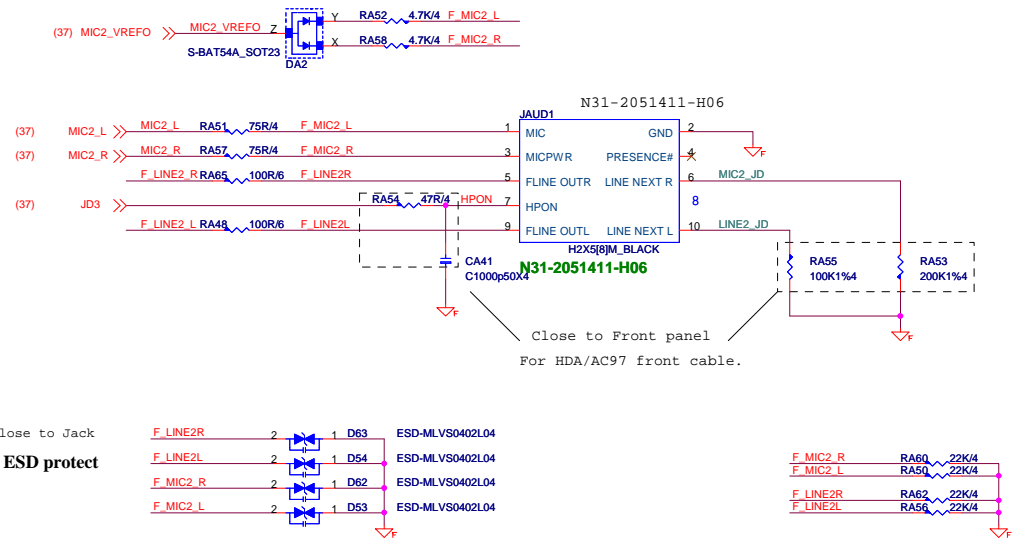
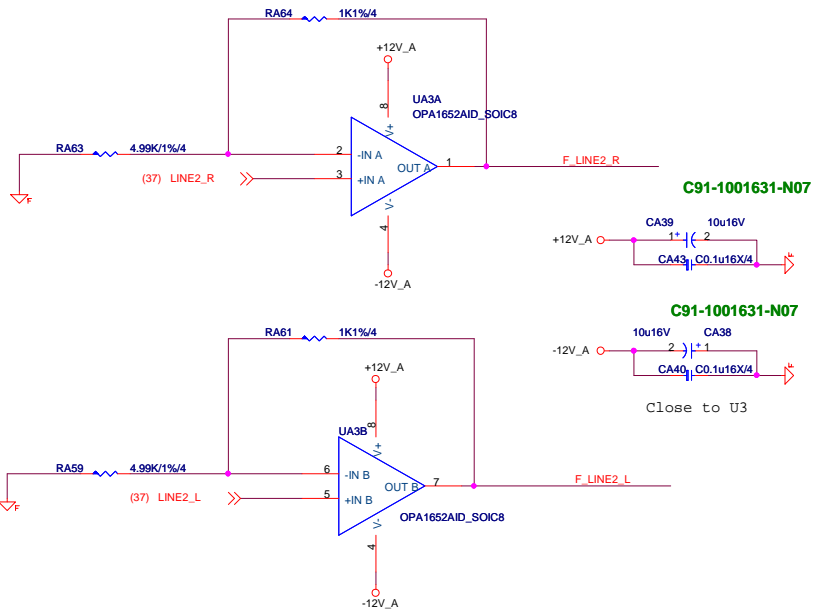
Size Custom	Document Description LAN - I211AT	Rev 1.2
Date: Monday, April 01, 2019	Sheet 36 of 75	

ALC1220P-VB2_48PIN

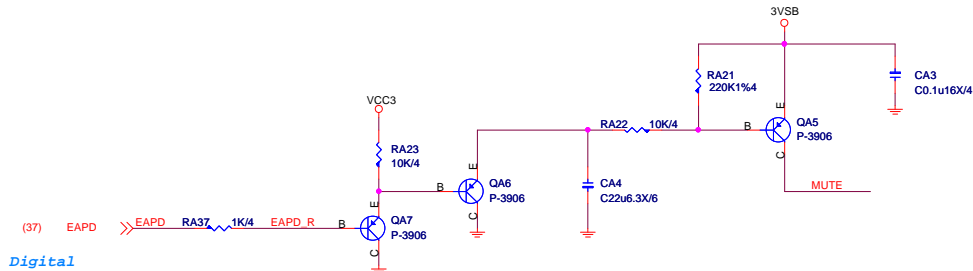


CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V

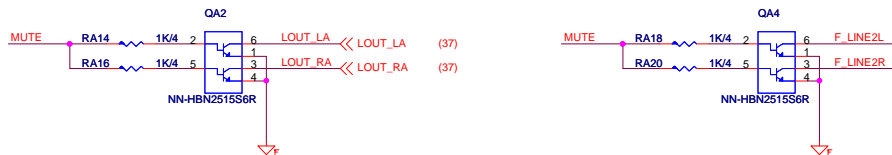




Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out & Front Headphone out)

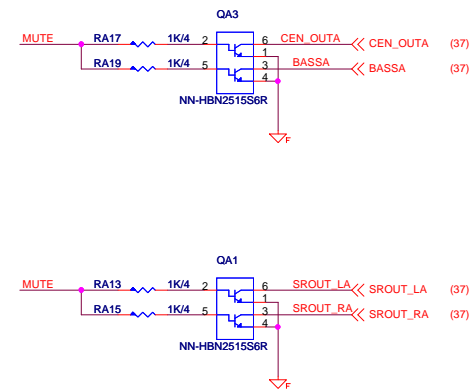


Analog

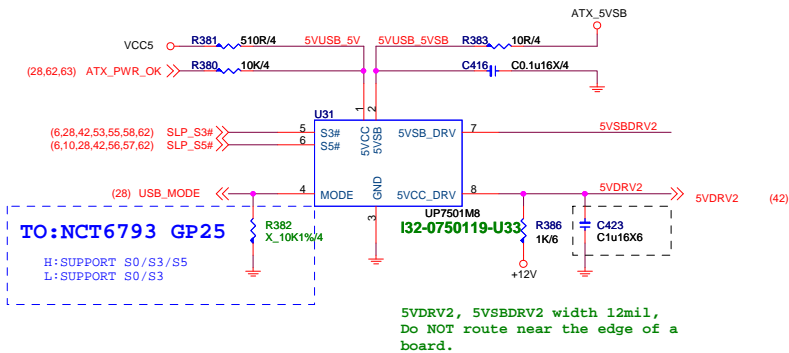


Audio moat is transparent and width 40mil

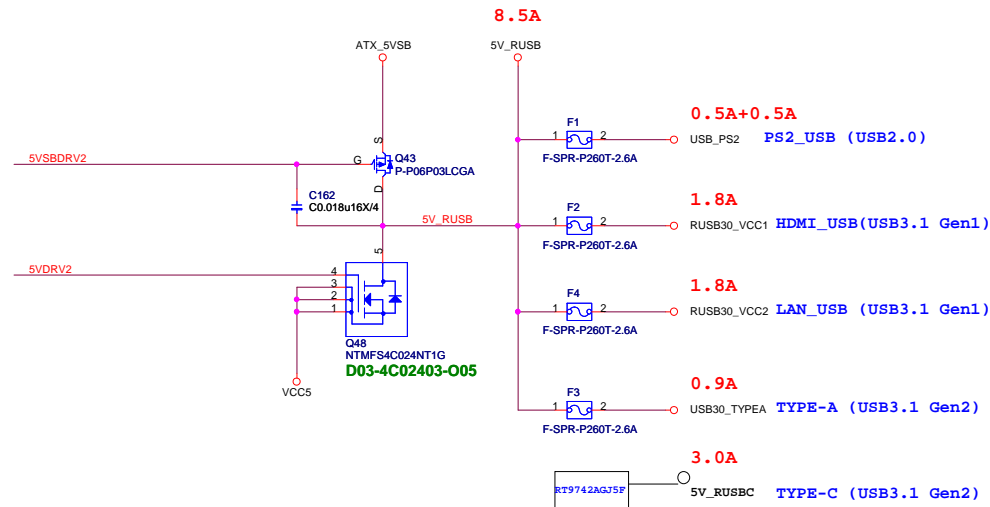
(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change SROUT_LA, SROUT_RA, CEN_OUTA, BASSA to TVS)



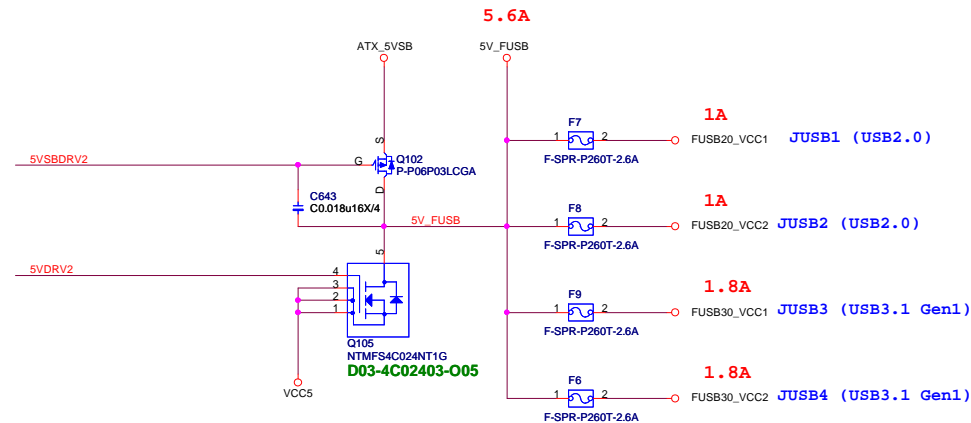
USB Power



Rear USB Port Power



Front USB Port Power

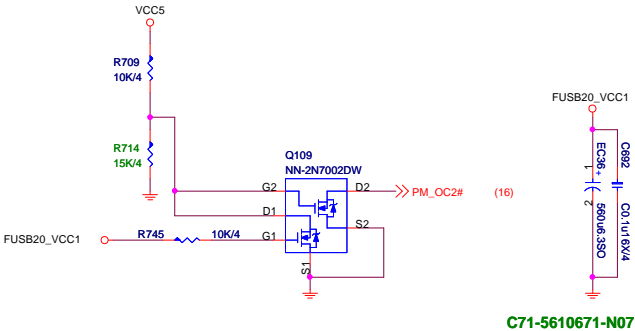
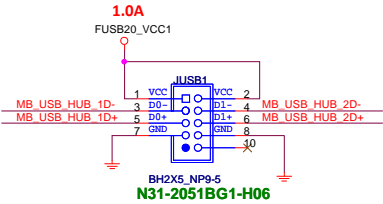
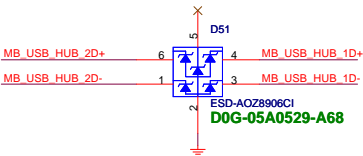


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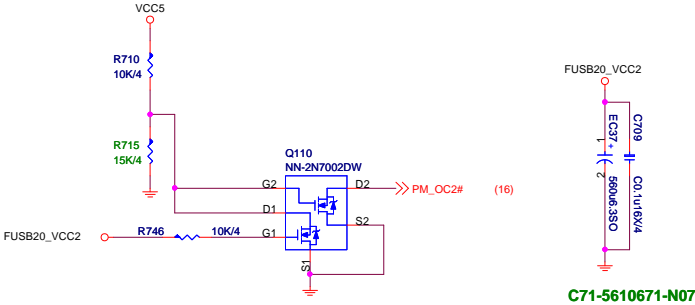
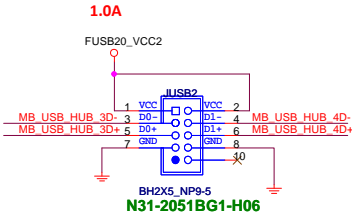
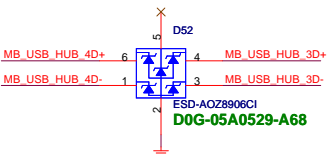
MS-7C37

Size	Document Description	Rev
Custom	USB Power - UP7501	1.2
Date: Monday, April 01, 2019		Sheet 39 of 75

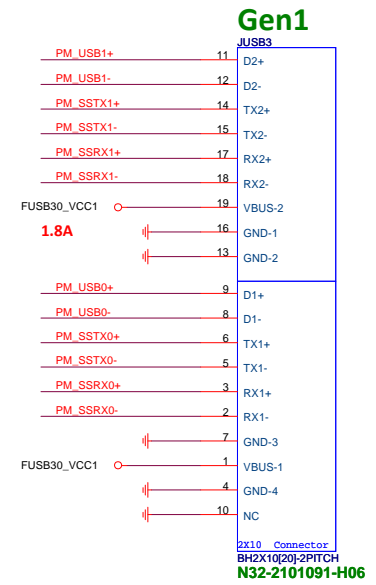
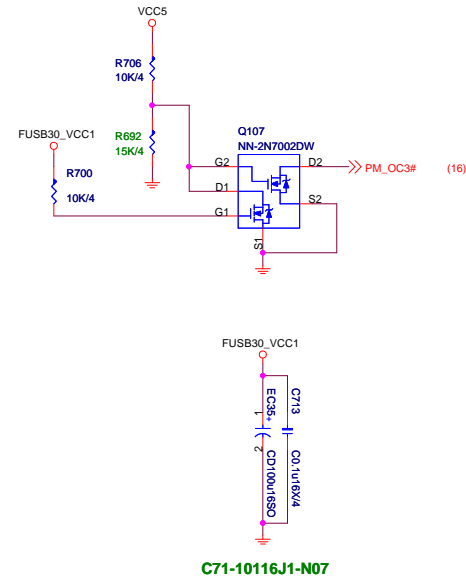
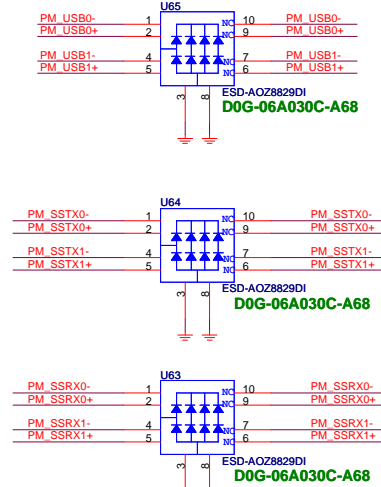
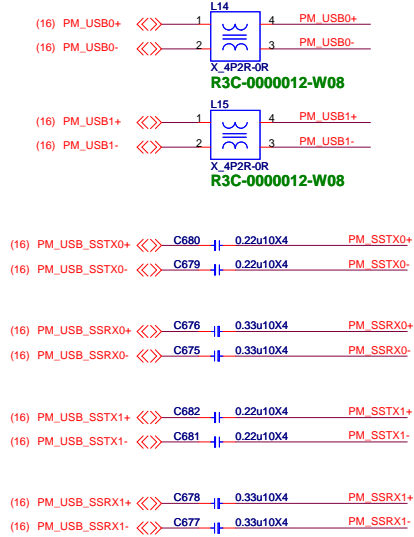
Front USB2.0(JUSB1)



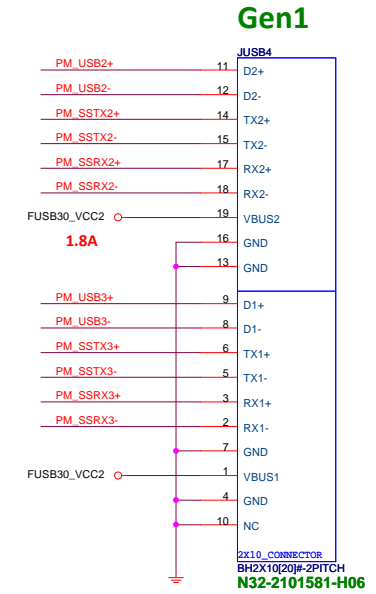
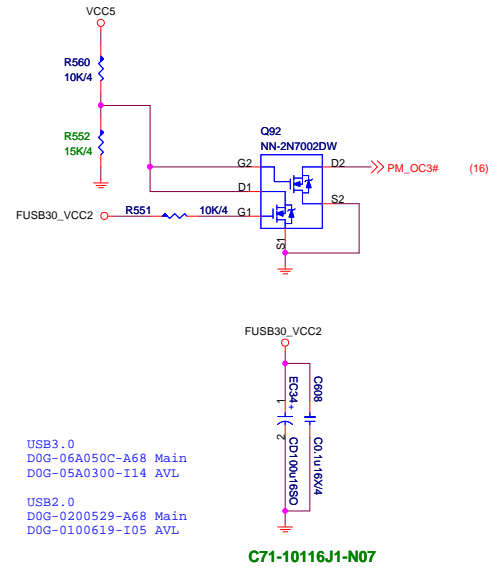
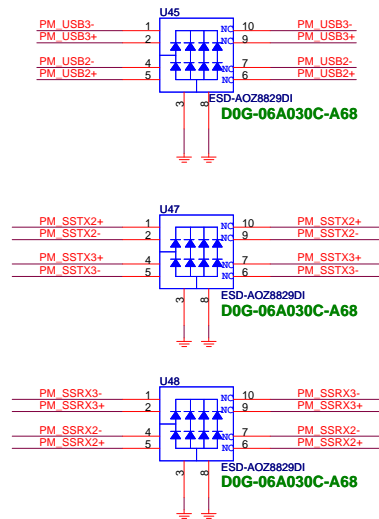
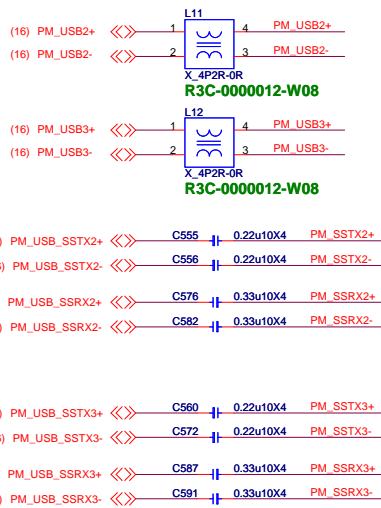
Front USB2.0(JUSB2)



Front USB3 180° BOX Header(JUSB3)



Front USB3 90° BOX Header(JUSB4)



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PS2

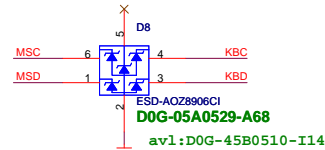
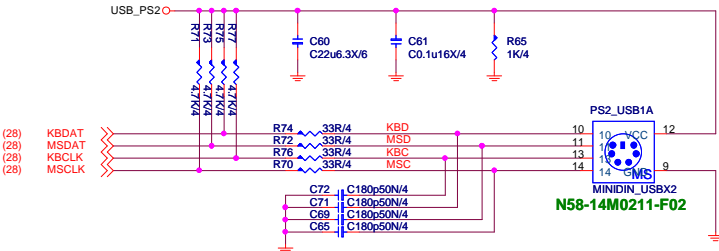
5V@1A

layout note:

C21 must close to TVS pin5

TVS must near KB_MS1 connector and route without branch

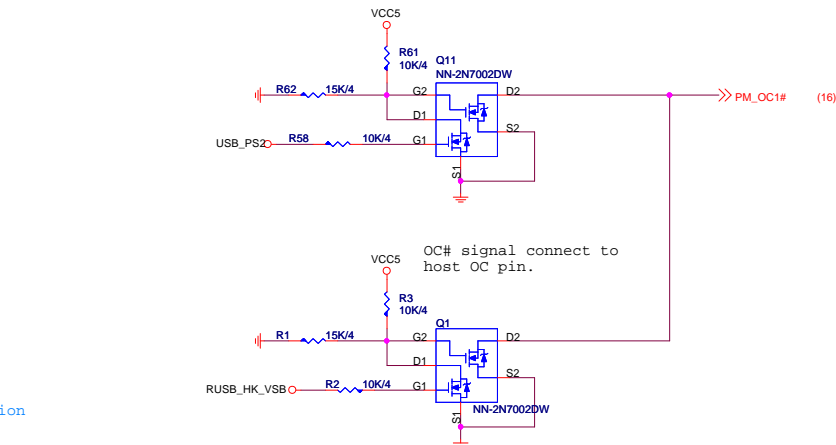
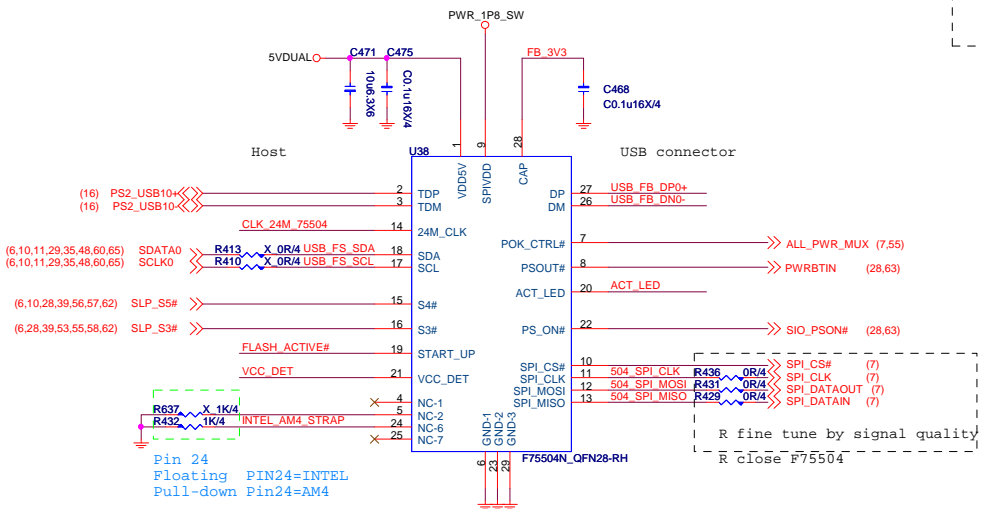
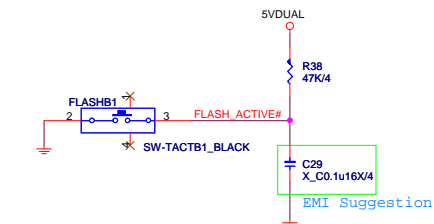
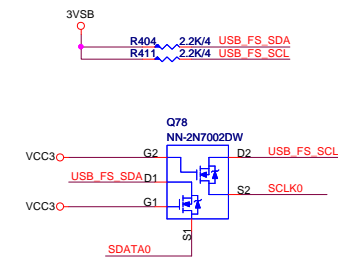
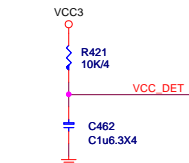
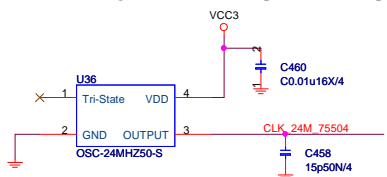
Varistor must close to TVS and route without branch



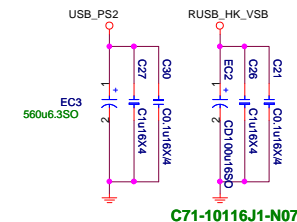
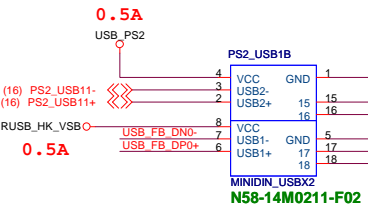
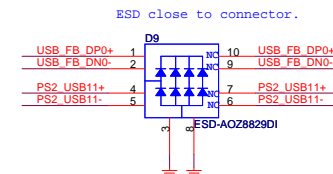
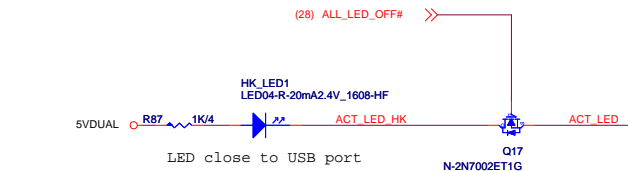
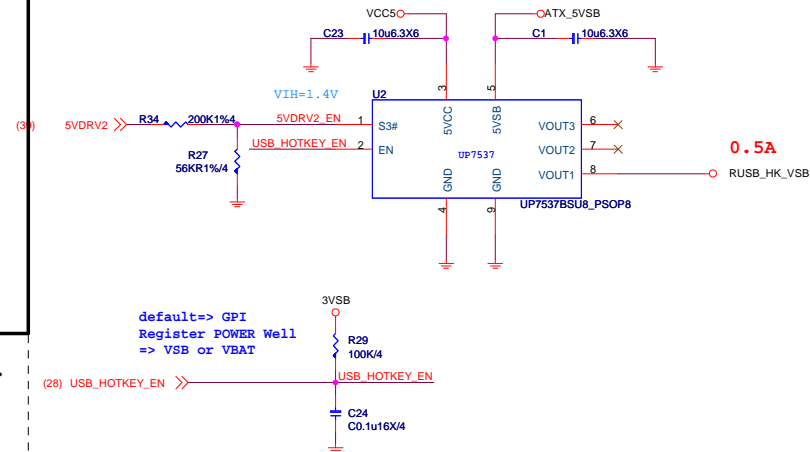
USB2.0 Flash BIOS

F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.

CLK running in S0,don't require in sleep



HOTKEY POWER

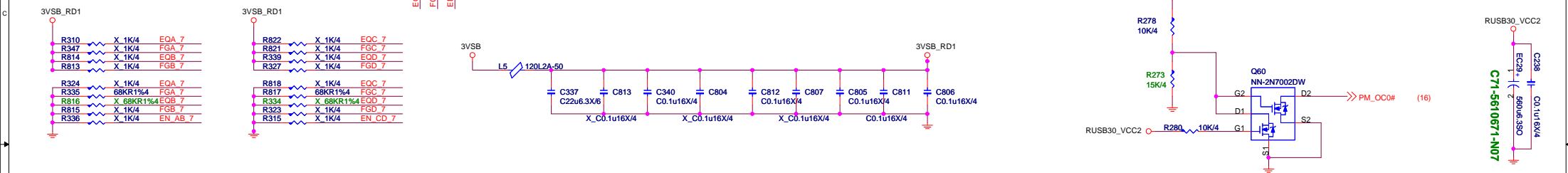
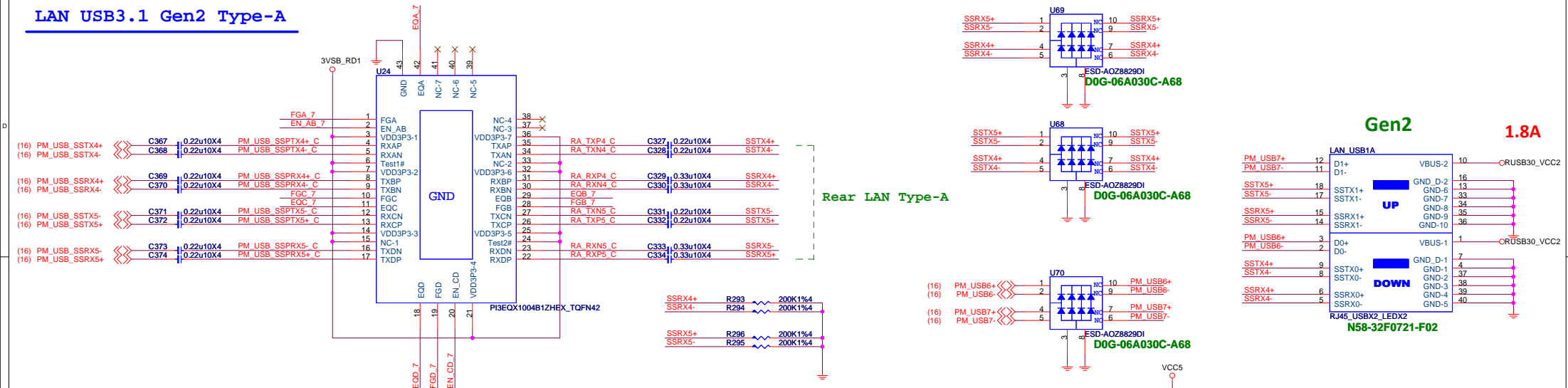


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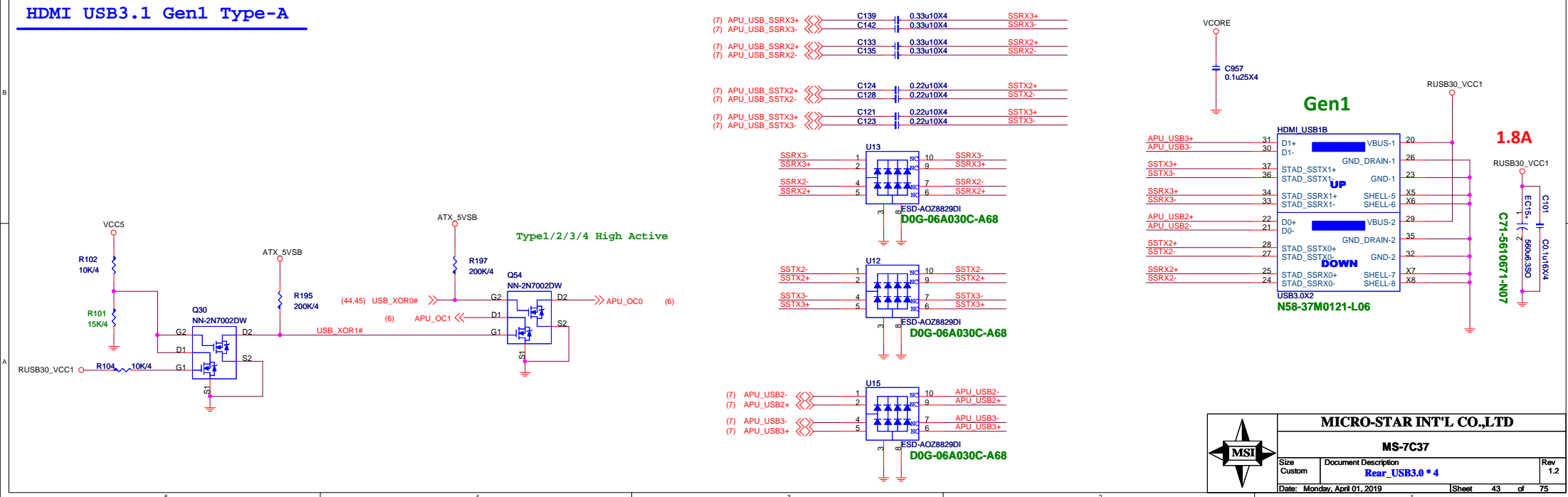
MS-7C37

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LAN USB3.1 Gen2 Type-A



HDMI USB3.1 Gen1 Type-A

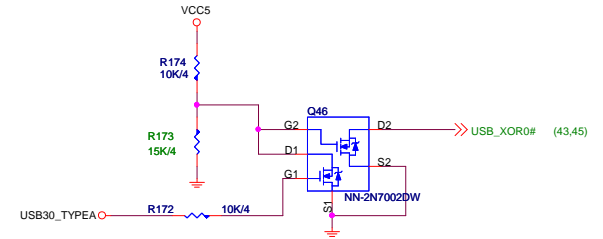
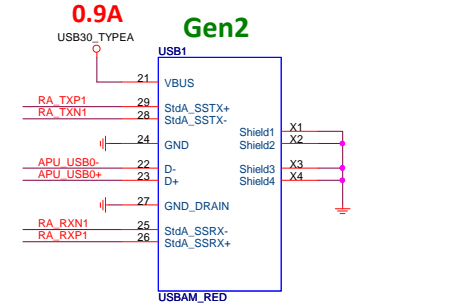
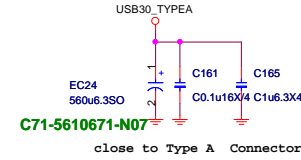
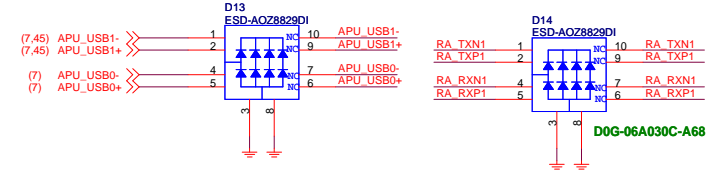
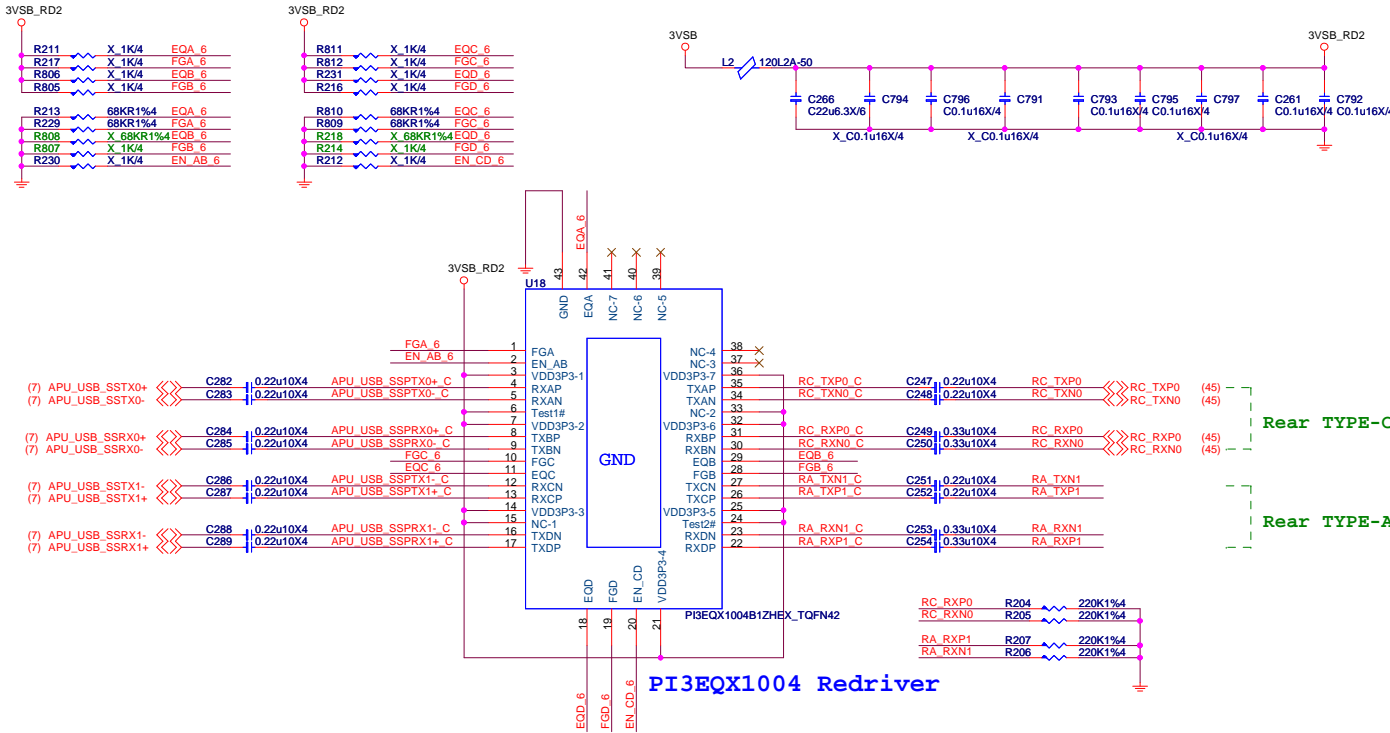


MICRO-STAR INT'L CO.,LTD

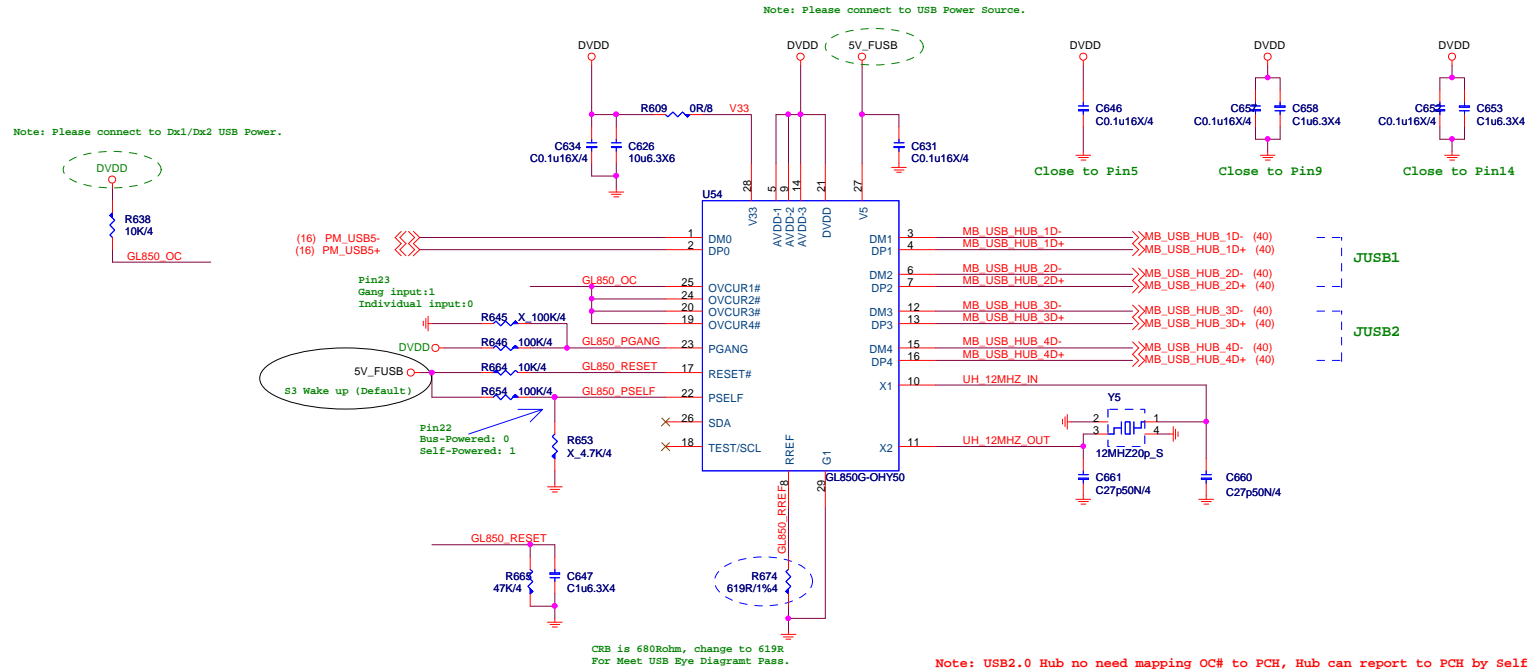
MS-7C37

Size Custom	Document Description Rear_USB3.0 * 4	Rev 1.2
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USB3.1 Gen2 Redriver + Type-A

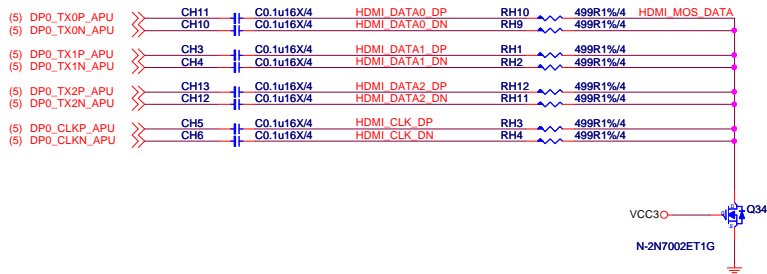


5V_FUSB



HDMI CONNECTOR

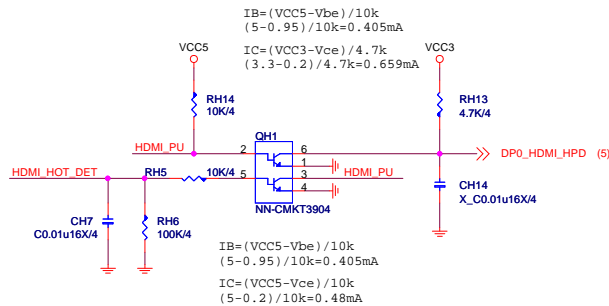
For HDMI 1.4



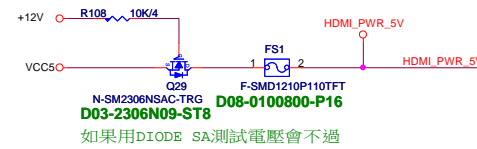
刪除RH6/RH12/RH15/RH16
For 增加VCC5寬度

For EMI

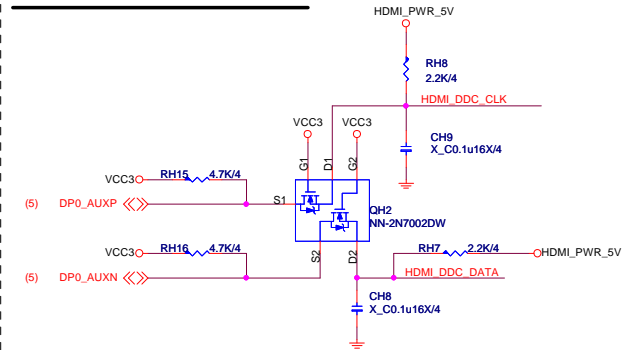
HPD Circuit



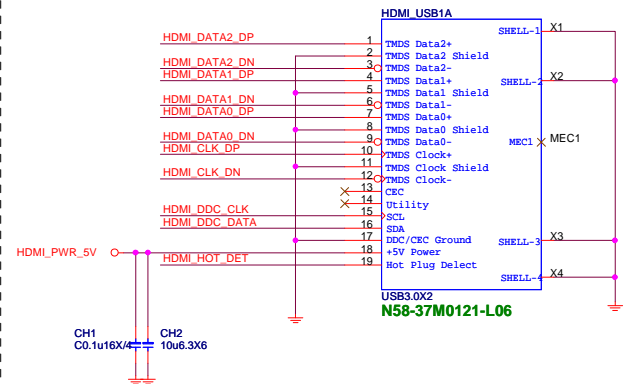
Connector Power



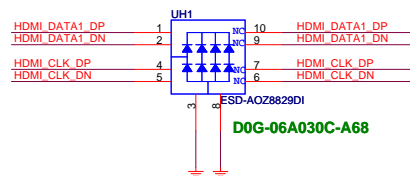
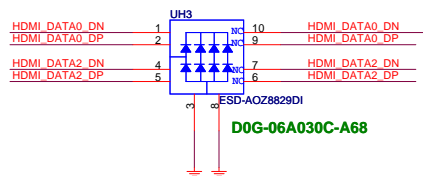
AUX Level Shifter



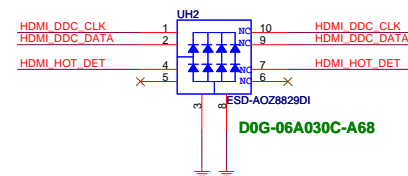
Connector

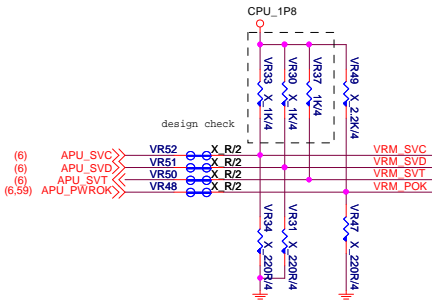


For EMI



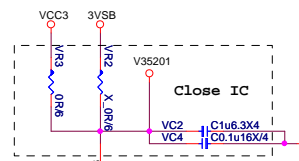
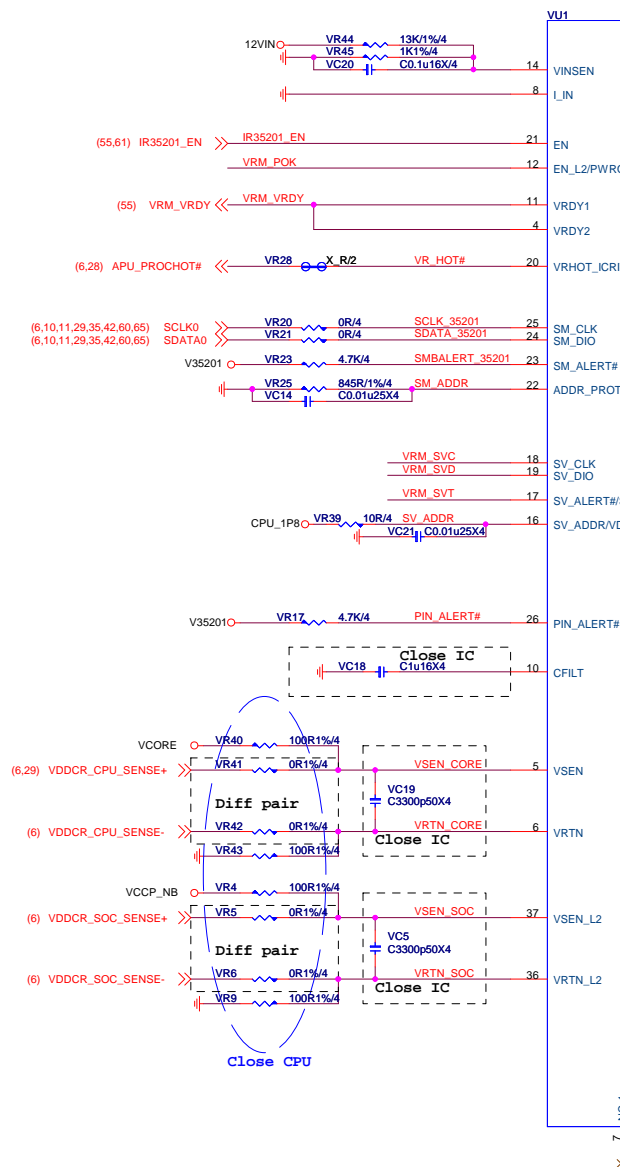
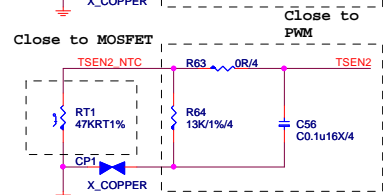
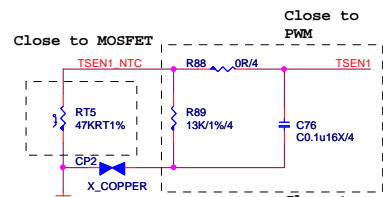
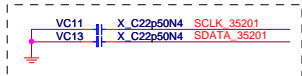
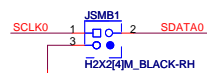
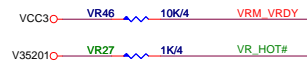
注意:耐壓5V零件



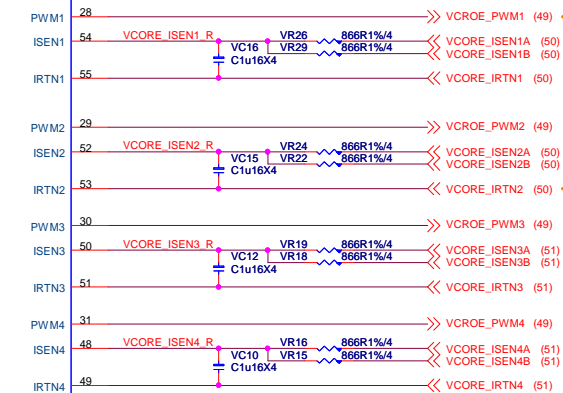


Note:VID Override Circuit

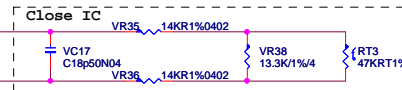
BOOT VOLTAGE		Pre_PWROK Metal VID
SVC	SVD	
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



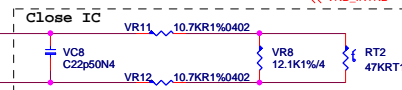
燒錄打點:IC正面上橋+金色點



Phase 1 close to CPU power pin.



RT close to Choke



RT close to Choke

0x26:RH=18K,RL=13K							
Default	VR53	VR54	VC20	VR58	VR57	VR59	VR60
Temp	6.49k	10k	100p	X	0R	X	0R
VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

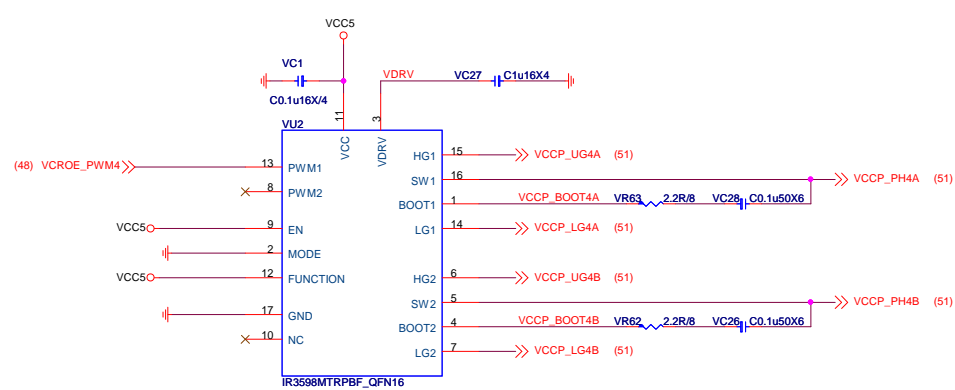
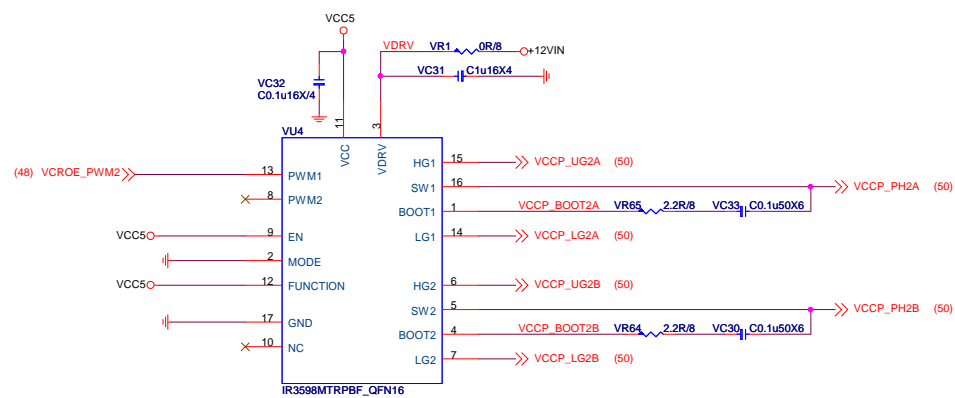
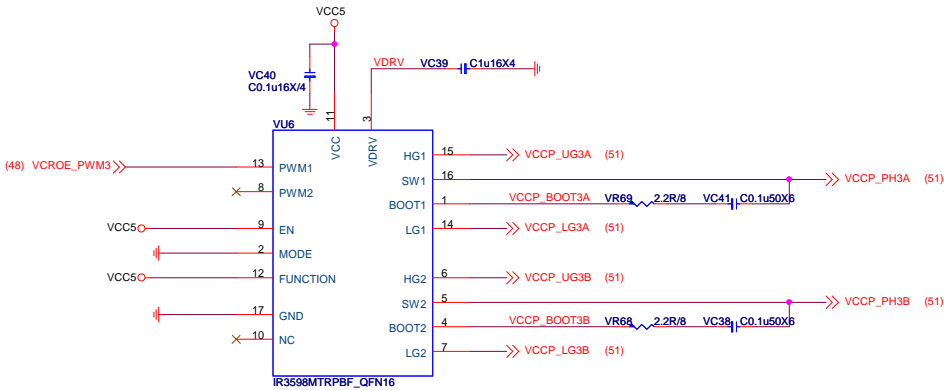
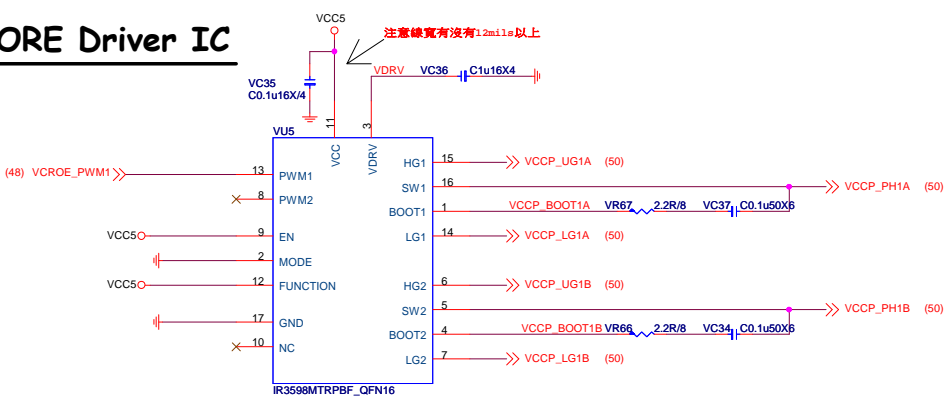


MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU Power IR35201 8+2	1.2
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CPU_CORE Driver IC



CPU_SOC Driver IC

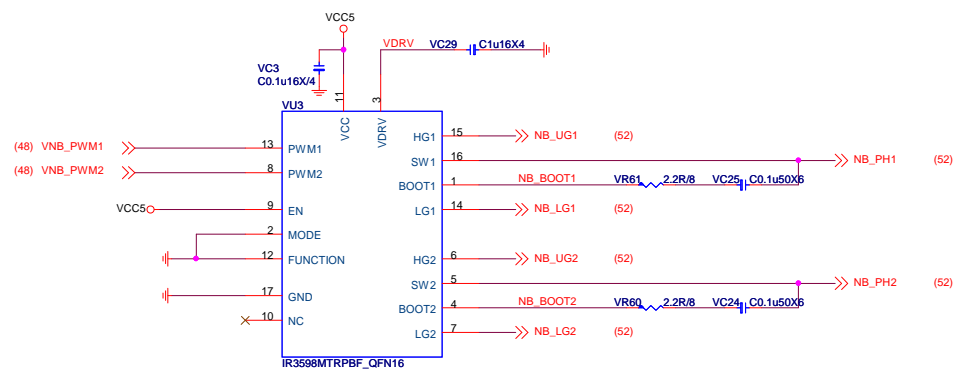
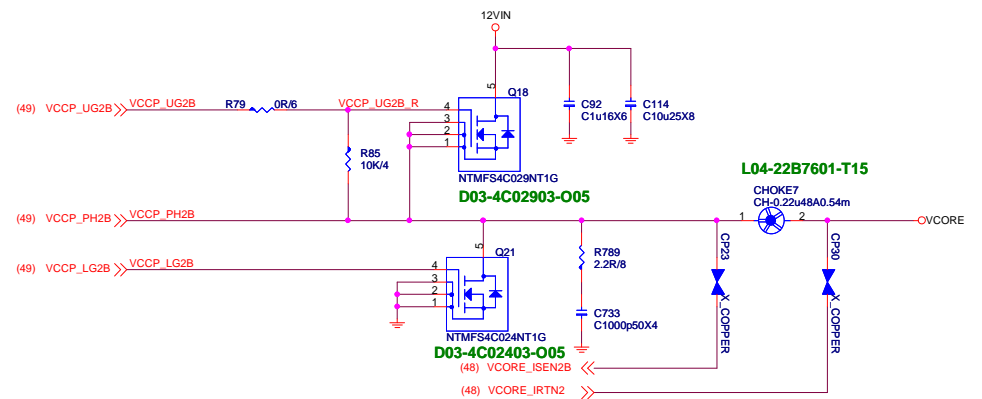
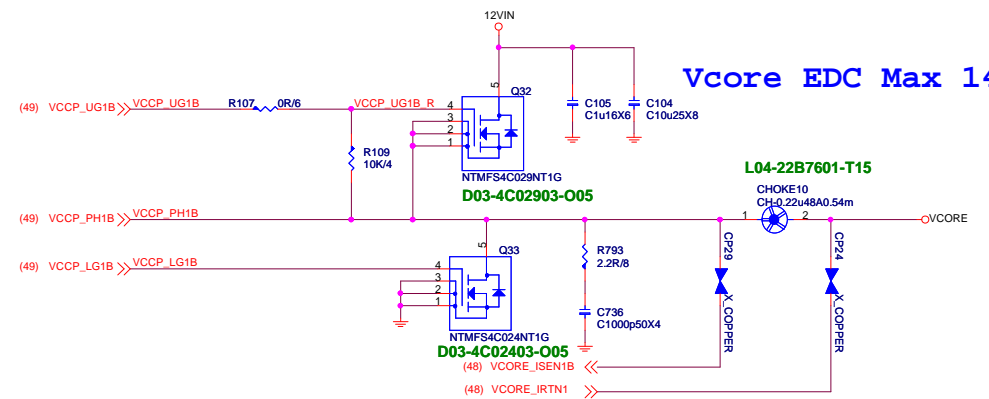


Table for IR3598				
Function	Mode	PWM Mode	Phase Mode	
0	1	IR ATL	Dual	
1	1	IR ATL	Doubler	
0	0	Tri-State	Dual	SOC
1	0	Tri-State	Doubler	Vcore

MICRO-STAR INT'L CO.,LTD

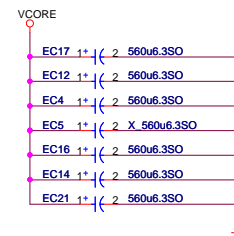
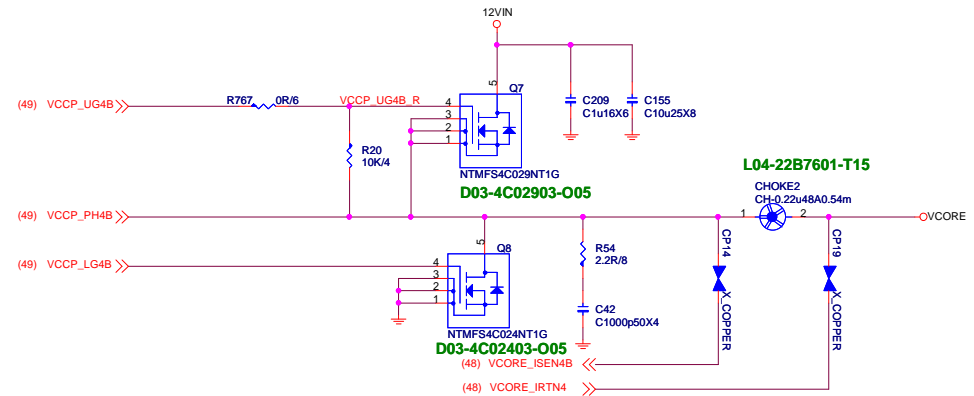
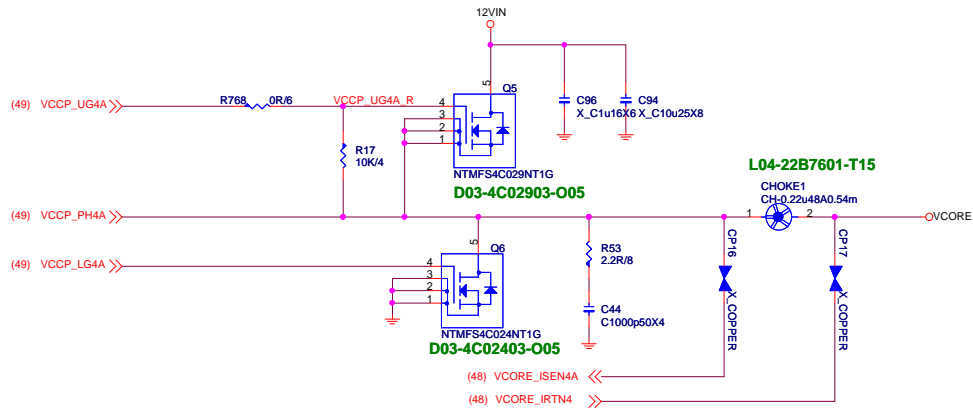
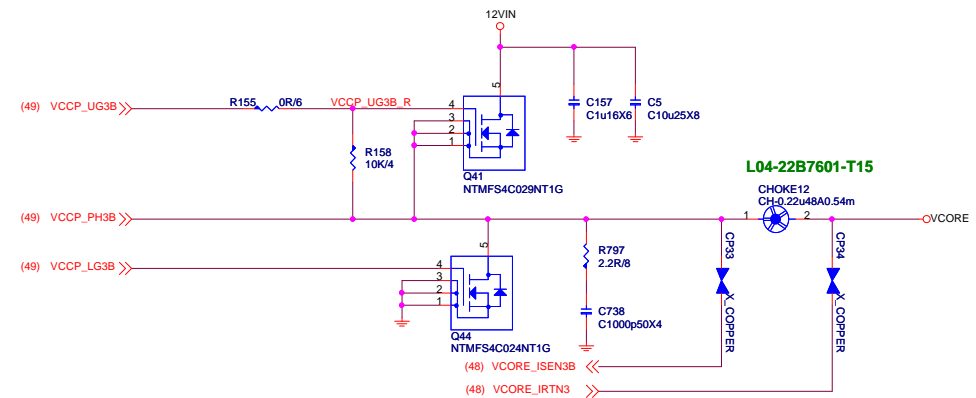
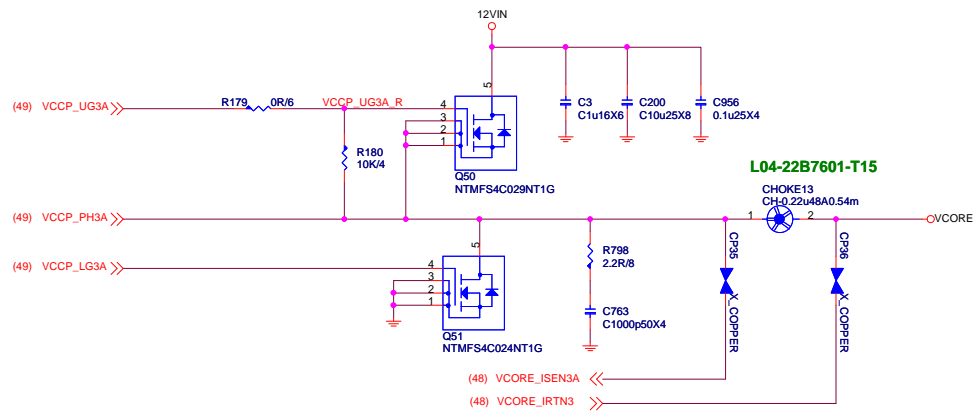
MS-7C37

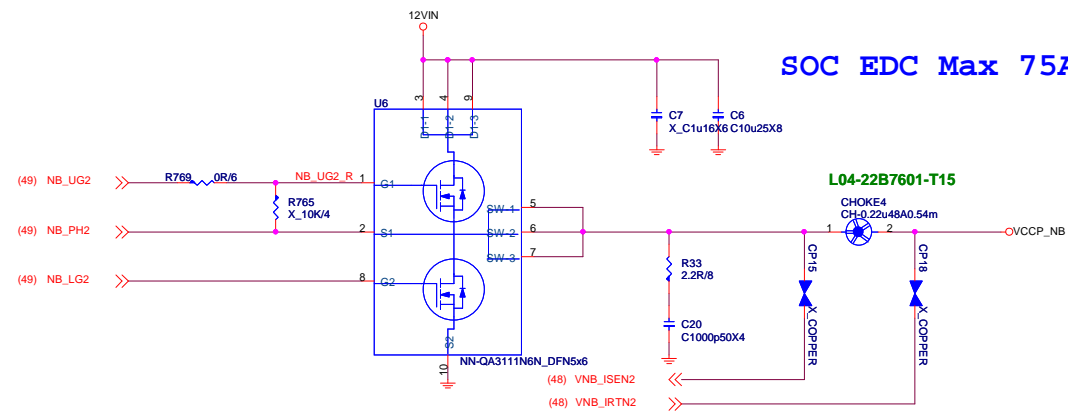
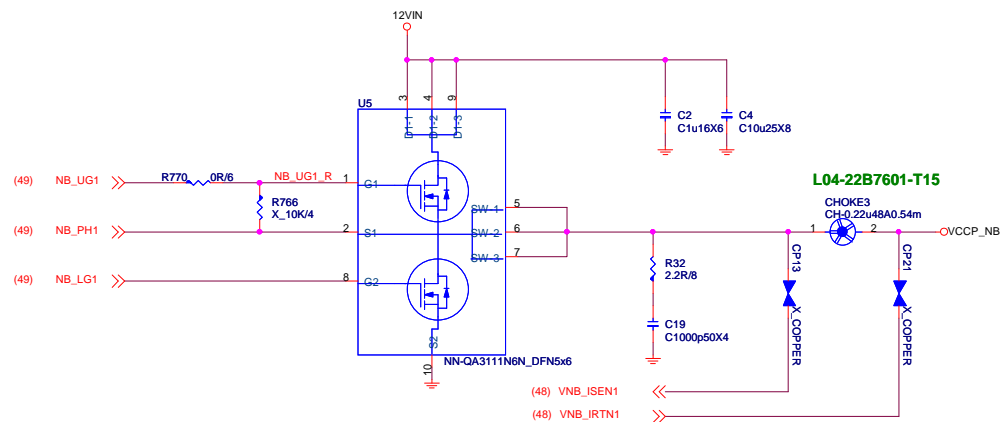
Size Custom	Document Description CPU Power Driver IC IR3598	Rev 1.2
Date: Monday, April 01, 2019	Sheet 49 of 75	



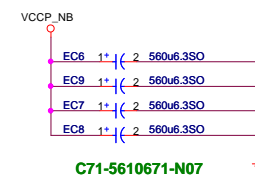
MS-7C37

Size Custom	Document Description CPU Power Vocre Phase 1-6	Rev 1.2
Date: Monday, April 01, 2019		Sheet 50 of 75





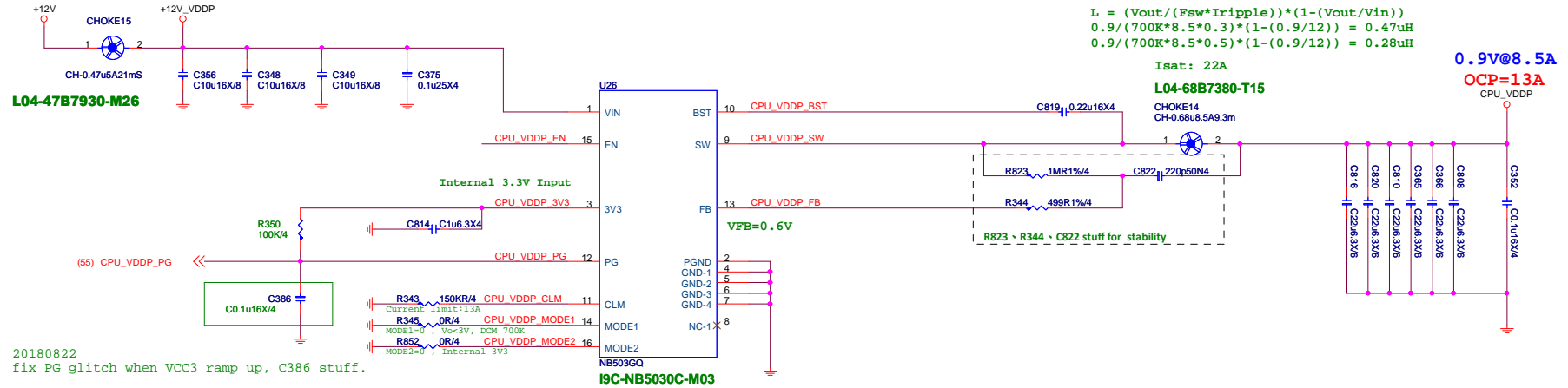
SOC EDC Max 75A



CPU_VDDP

CPU: VDDP@8.5A

Input Current = $(8.5A \cdot 0.9V) / 12V / 0.8 = 0.8A$
Choke Isat = 8A
 $I_{rms} = I_{out} \cdot \sqrt{(V_o/V_i) \cdot (1 - (V_o/V_i))}$
 $= 13 \cdot \sqrt{(0.9/12) \cdot (1 - (0.9/12))} = 3.42A$
Choke I_{rms} = 5A

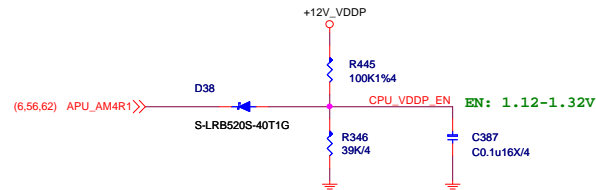
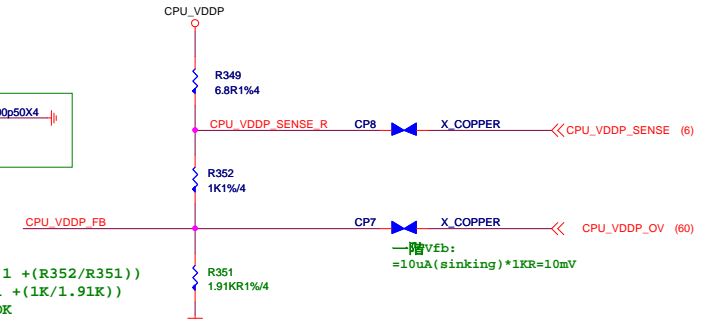


No support BR SPEC

TYPE0_CPU_SEL
0:RV
1:BR/SR/PR/MTS

CPU_VDDP_EN:
X: BR/SR/PR/MTS
O: RV

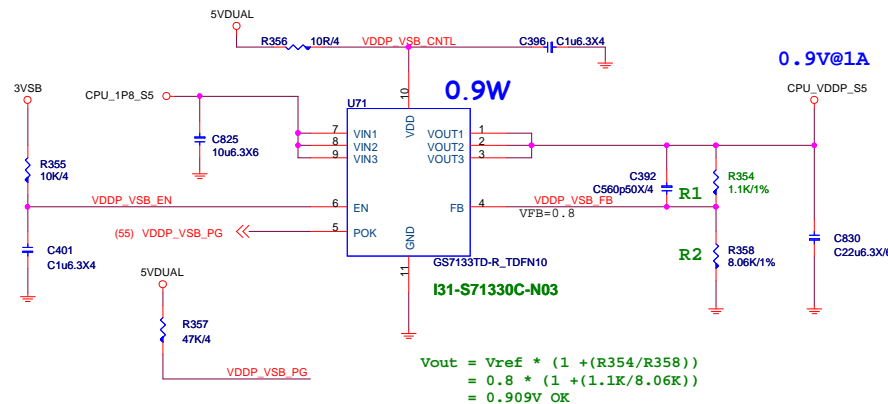
CPU_VDDP_EN (53)



$$V_{out} = V_{ref} * (1 + (R_{352}/R_{351}))$$
$$= 0.6 * (1 + (1K/1.91K))$$
$$= 0.914V \text{ OK}$$

CPU_VDDP_S5

CPU: VDDP_S5@1A



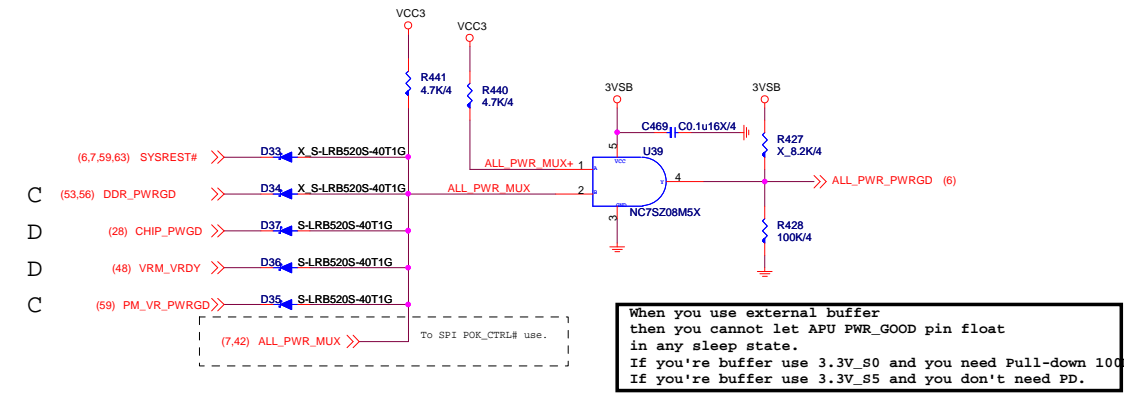
MICRO-STAR INT'L CO.,LTD

MS-7C37

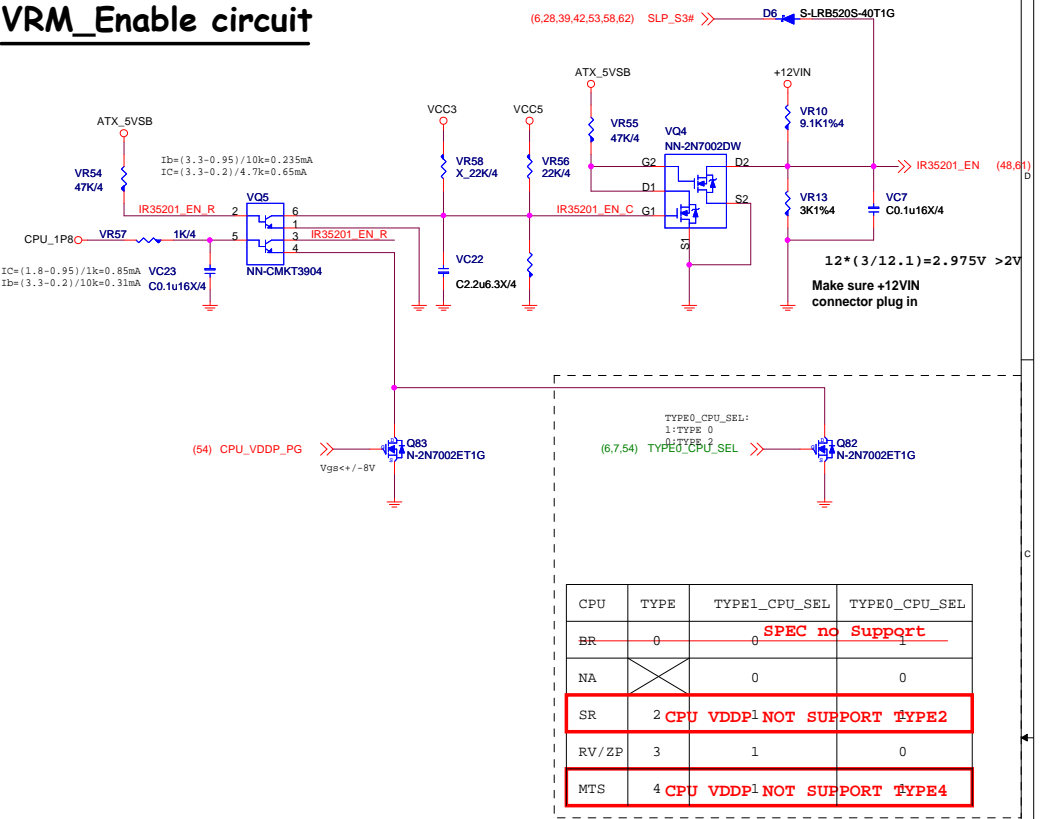
Size	Document Description	Rev
Custom	CPU Power VDDP - NB503	1.2
Date:	Monday, April 01, 2019	Sheet 54 of 75

ALL POWER GOOD MUX

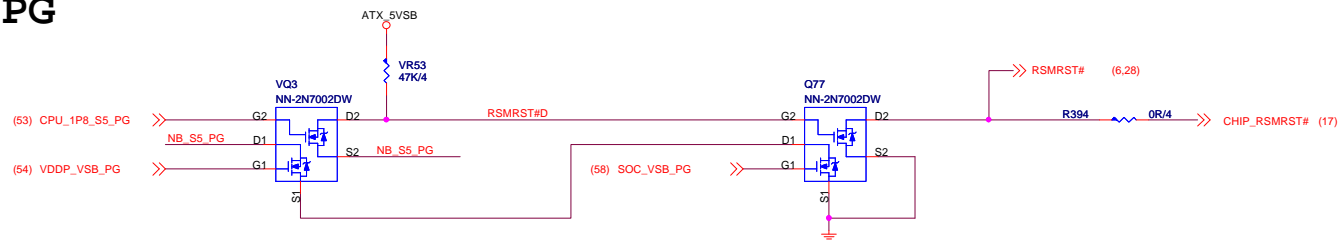
S0 PG



VRM_Enable circuit

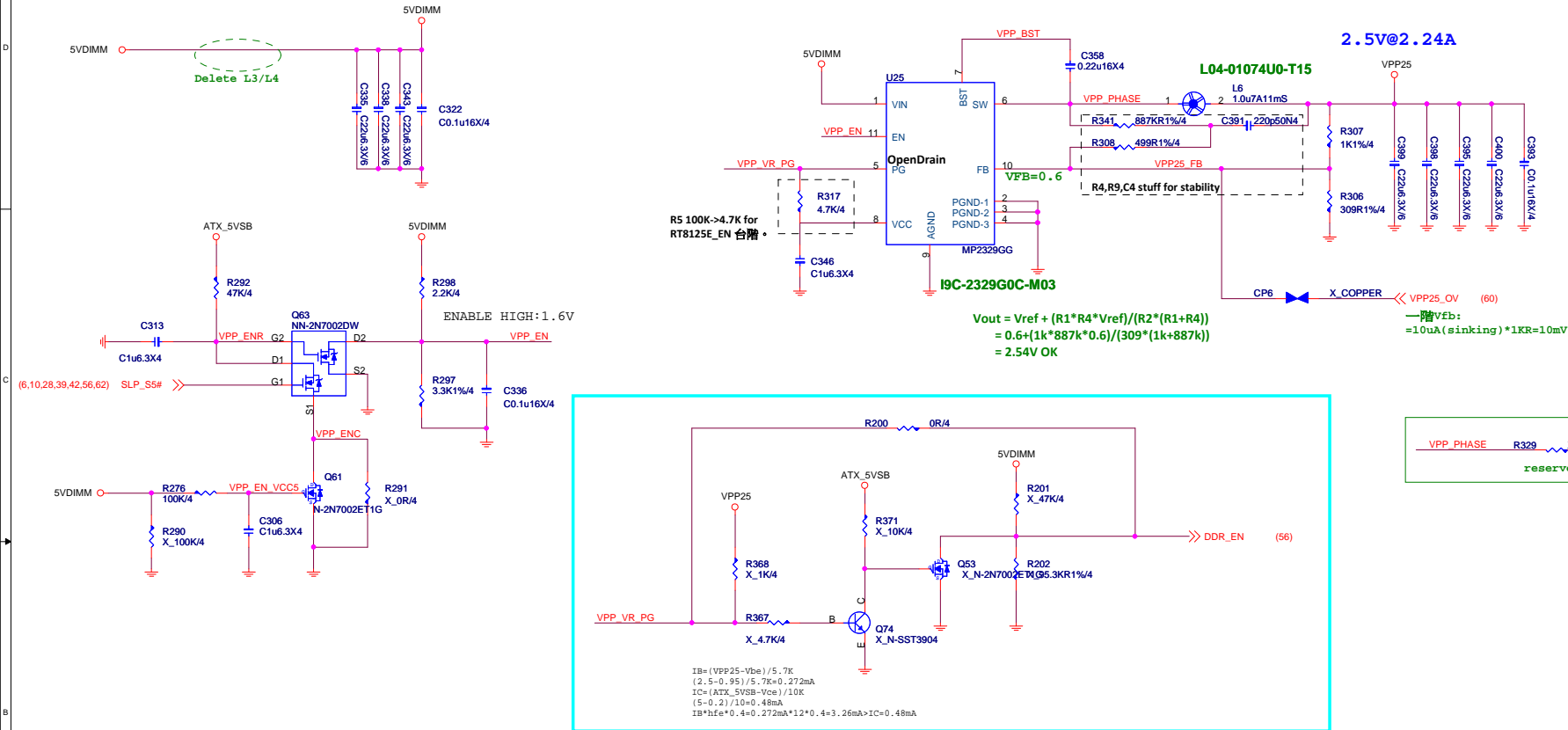


S5 PG



VPP25

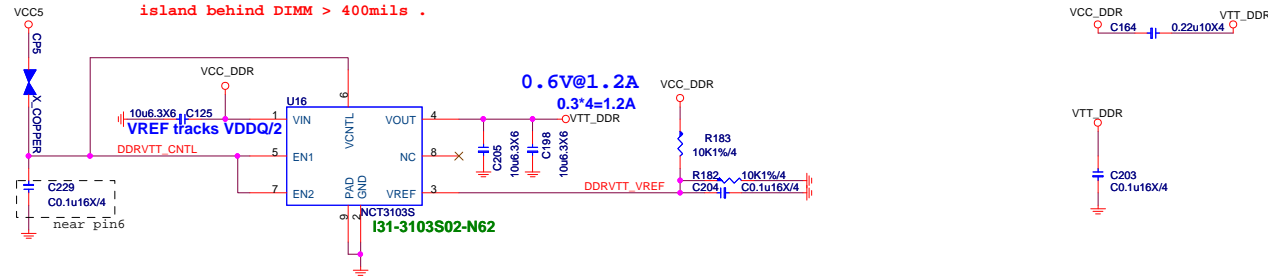
2.5V@2.24A



VTT_DDR

0.6V@1.2A

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



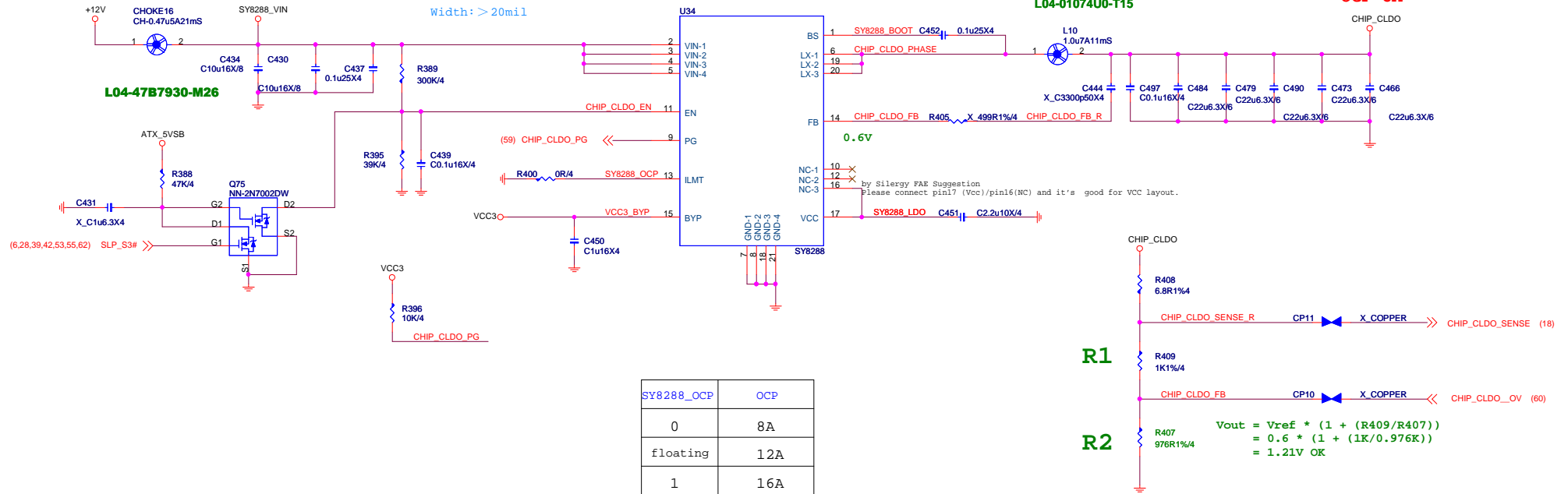
MICRO-STAR INT'L CO.,LTD			
MS-7C37			
Size	Document Description	Rev	
Custom	DDR VPP25 / VTT	1.2	
Date:	Monday, April 01, 2019	Sheet	57 of 75

CHIP_CLDO

CHIP: VDD_CLDO@5A

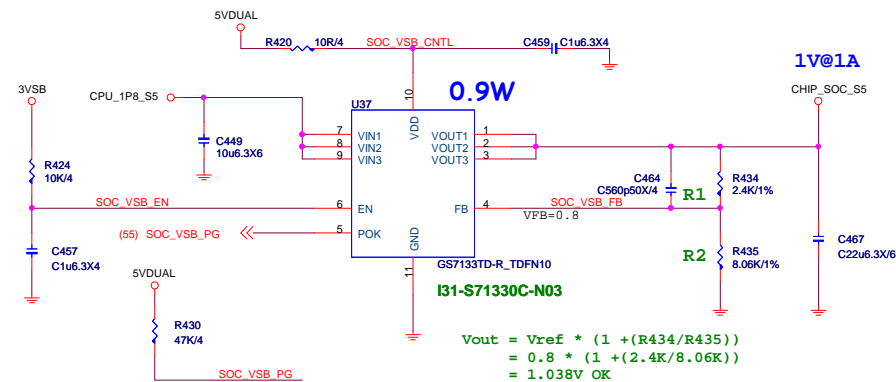
Input Current= (5.5A*1.05V)/12V/0.8=0.625A

1.2V@5A
OCP=8A



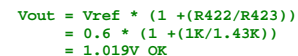
CHIP_SOC_S5

CHIP: VDDCR_SOC_S5@1A



CHIP: VDDCR SOC@9A

```
L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
1/(700K*12*0.3)*(1-(1/12)) = 0.432uH
1/(700K*12*0.5)*(1-(1/12)) = 0.218uH
```



VCC3
CHIP_CLDO
DDR_PWRGD
CPU_VDDP
CPU_1P8
CHIP_SOC

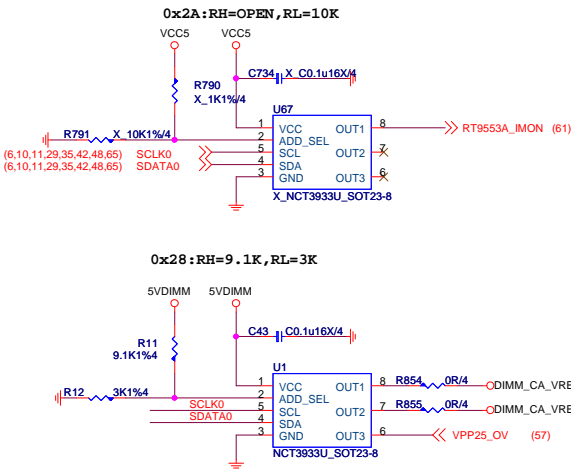


MICRO-STAR INT'L CO.,LTD

MS-7C37

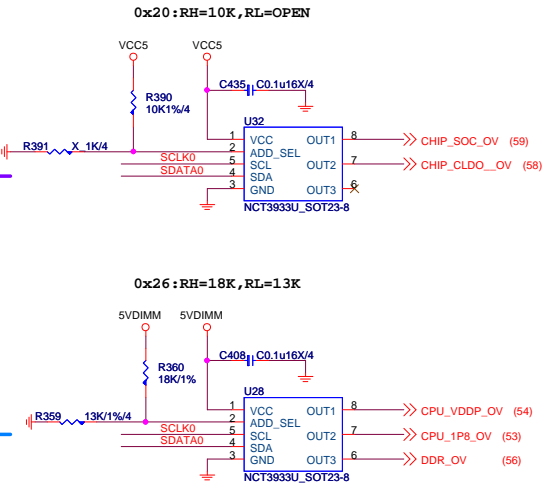
Size Custom	Document Description PROM - NB503 / 1.0V	Rev 1.2
Date: Monday, April 01, 2019		Sheet 59 of 75

Over Voltage Control IC



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

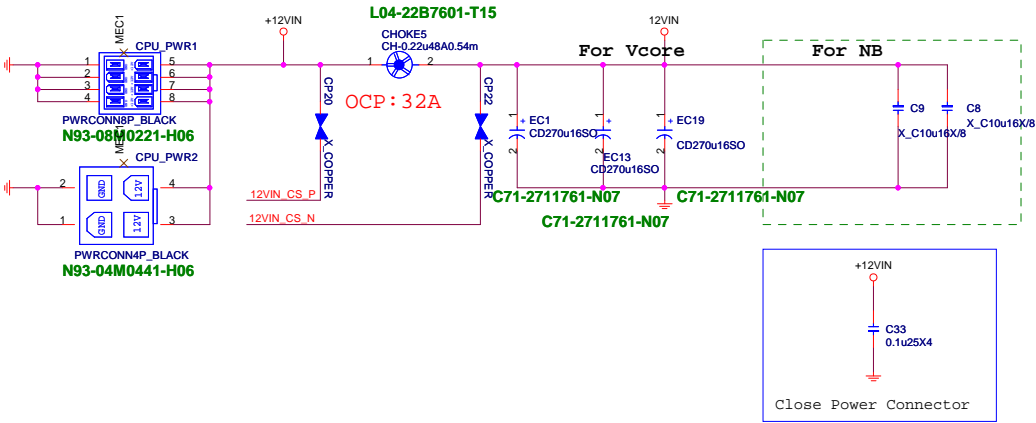


UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

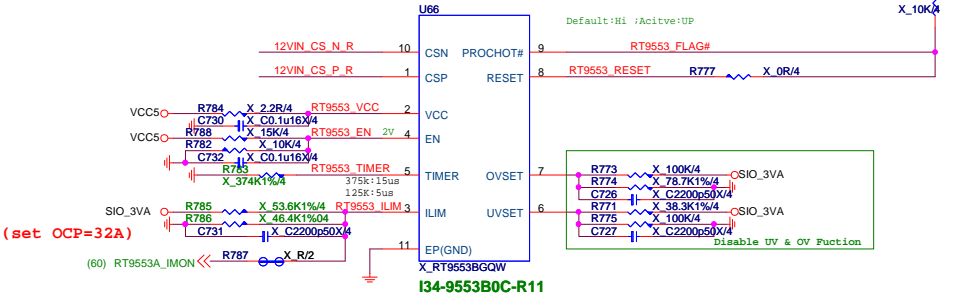


CPU POWER CONNECTOR

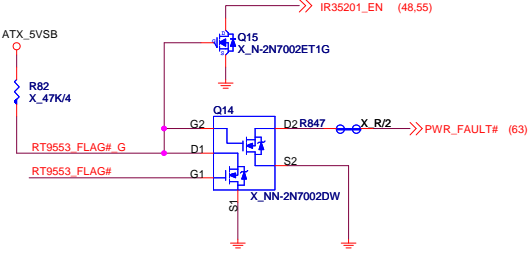
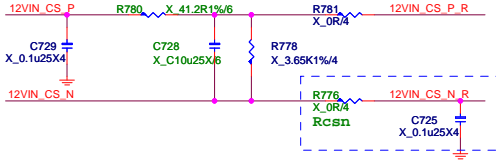


RT9553B CURRENT SENSE

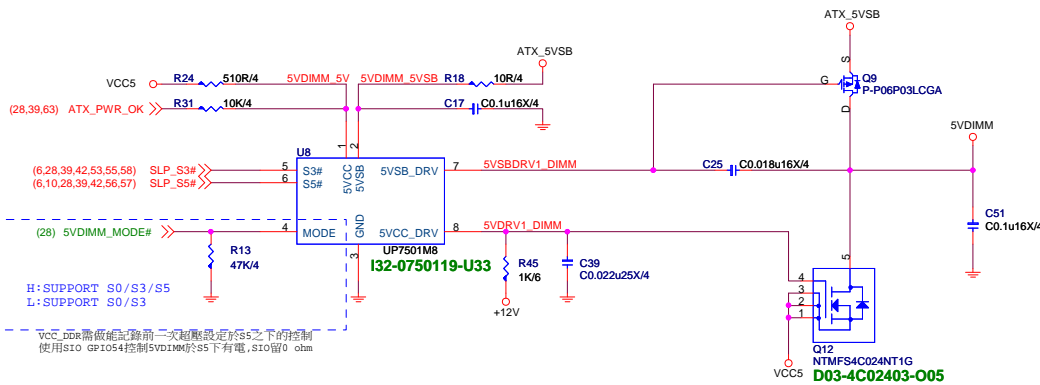
RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.



Vcore		SOC	
D=Vout/Vin		D=Vout/Vin	
Vin = 12	> input voltage	Vin = 12	> input voltage
Vout = 2	> output Vcore	Vout = 1.55	> output Vcore
D = 0.166667		D = 0.129167	
Io = Icore(max)*0.8		Io = Icore(max)*0.8	
I core(max) = 200	> Vcore current	I core(max) = 75	> Vcore current
I avg. = 160	A	I avg. = 60	A
I ripple={ Io*√D*√(1-D) } / Phase		I ripple={ Io*√D*√(1-D) } / Phase	
Phase = 10	phase	Phase = 2	phase
I ripple = 5.962848	A	I ripple = 10.06153	A
How many pcs. Of Cap.		How many pcs. Of Cap.	
I ripple(cap) = 4700	m A	I ripple(cap) = 4700	m A
COETEMP = 1		COETEMP = 1	
Input Cap. = 2	pcs.	Input Cap. = 3	pcs.



5VDIMM FOR DDR



teknisi indonesia

3VSB cost down

3.3V@3.363A

CPU: VDD_33_S5@0.25A

CHIP: VDD_33_S5@0.1A

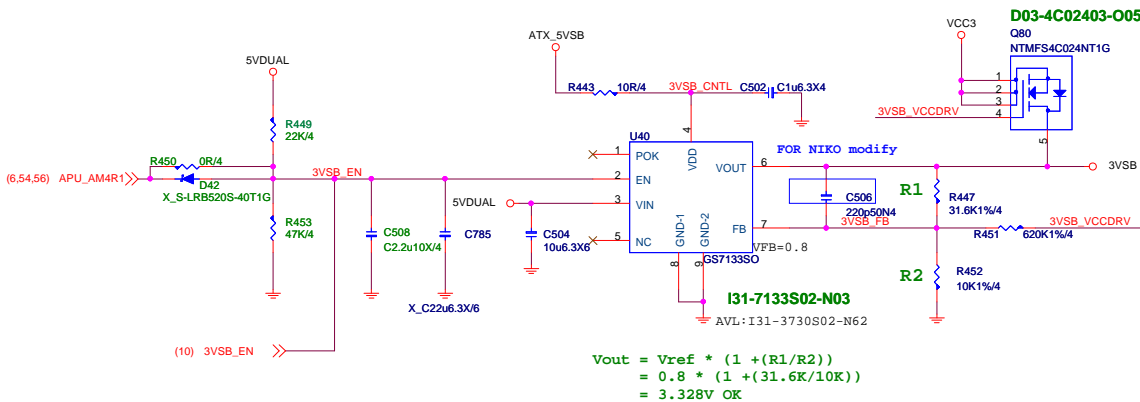
PCIE*4@1.5A

M.2_WIFI@0.78A

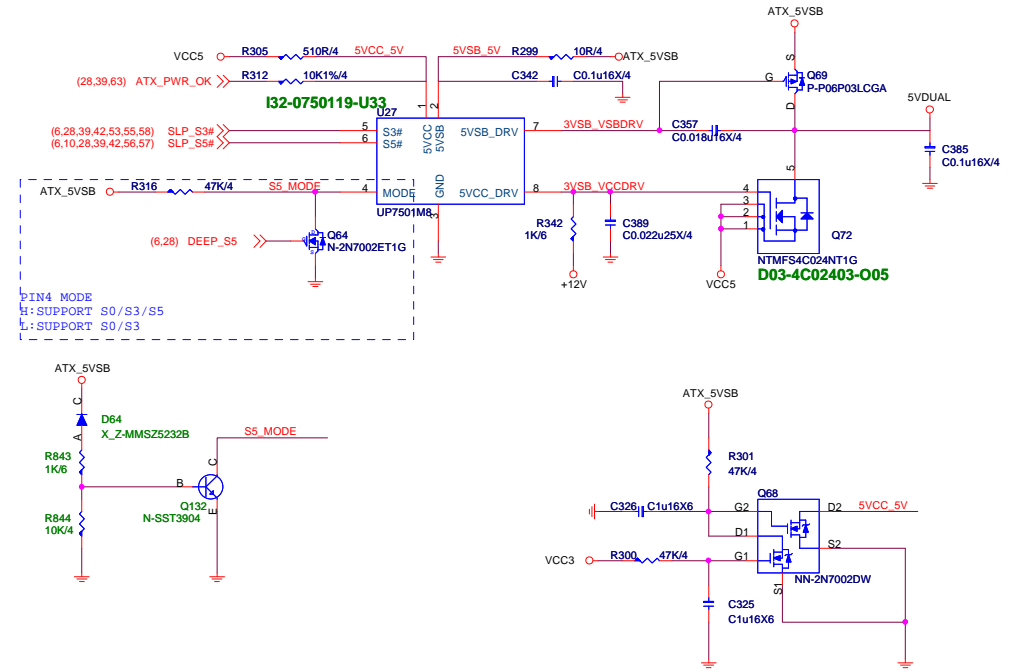
LAN@0.065A

Redriver*2@0.668A

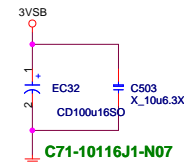
USB TYPE-C@0.9mA



5VDUAL For 3VSB、CPU 1.8V、VDDP

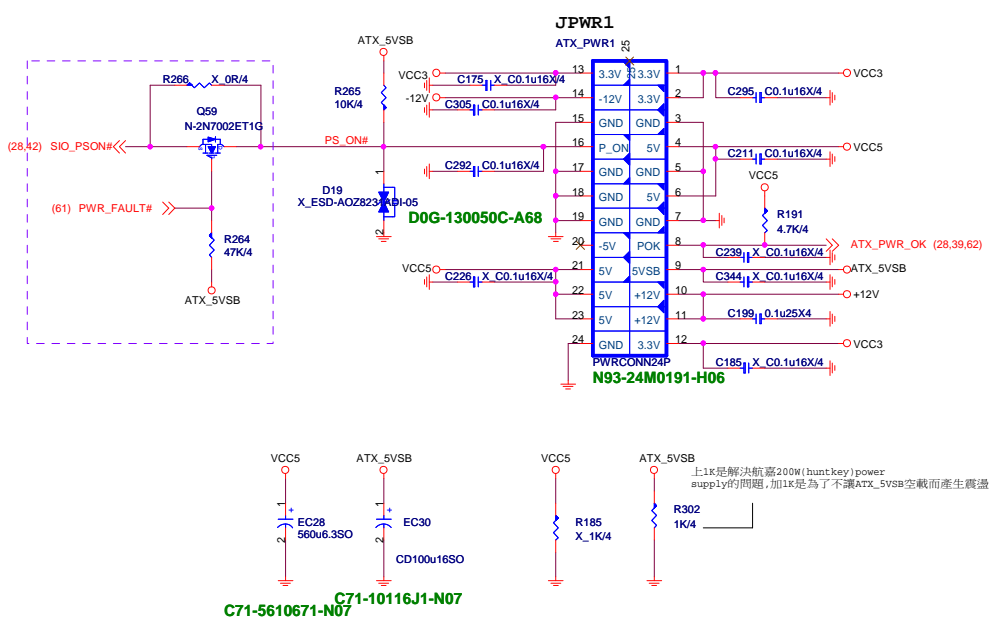


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

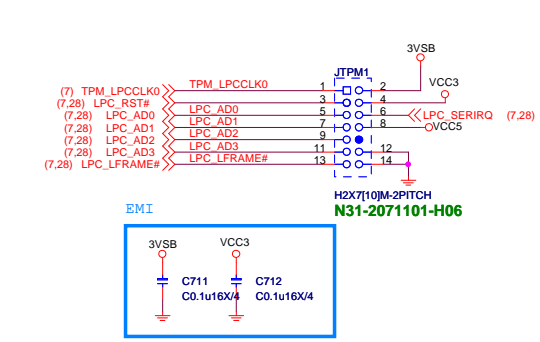


MICRO-STAR INT'L CO.,LTD			
MS-7C37			
Size	Document Description		Rev
Custom	ACPI - 3VSB / 5VDIMM		1.2
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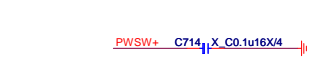
ATX POWER CONNECTOR



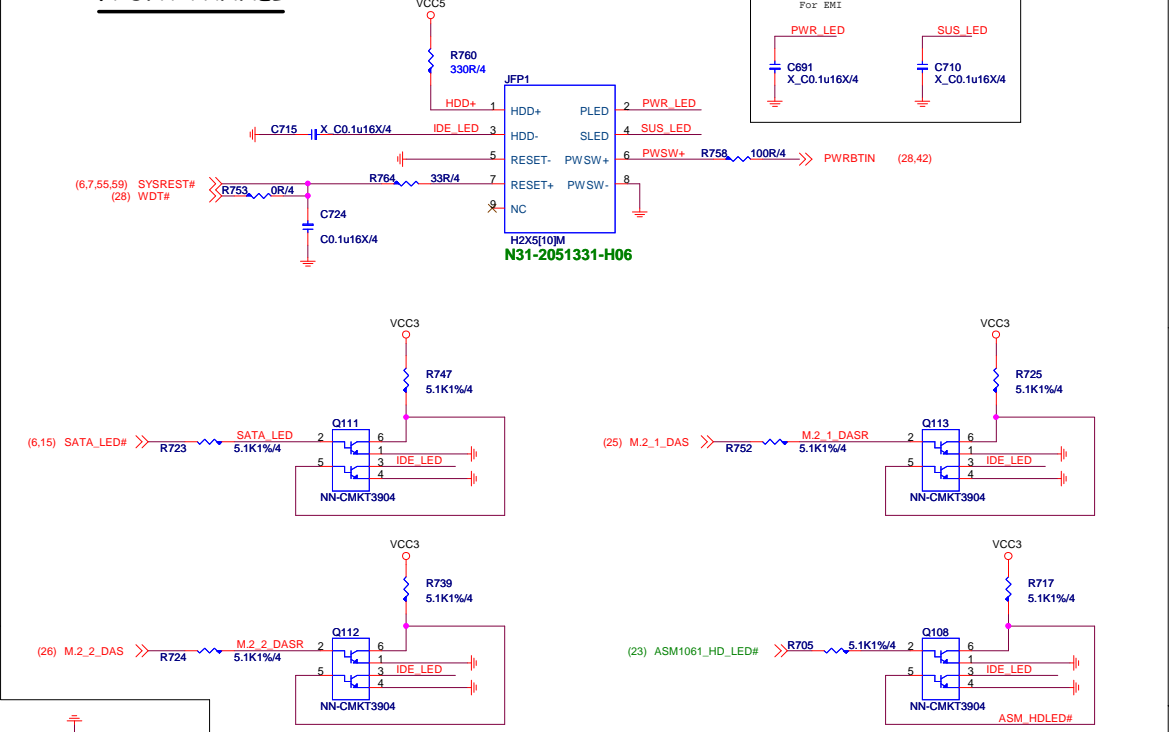
TPM



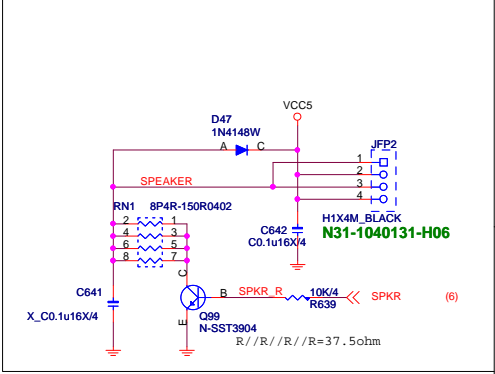
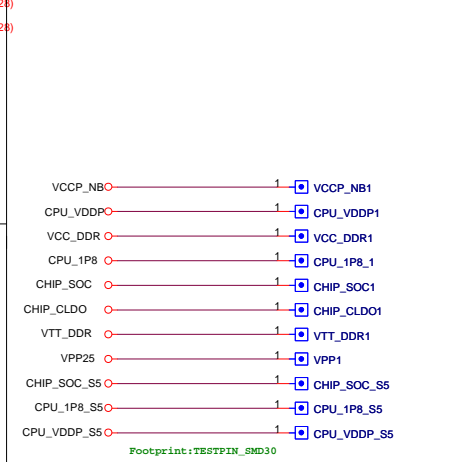
Add for EMI



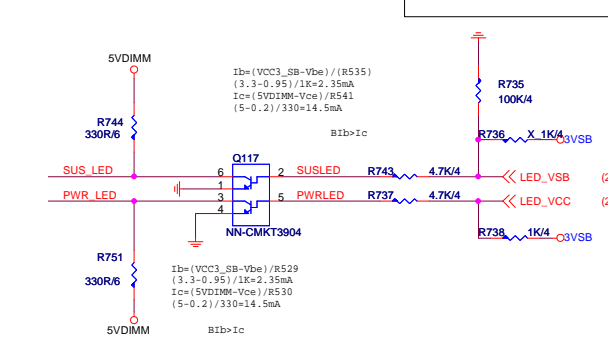
FRONT PANNEL



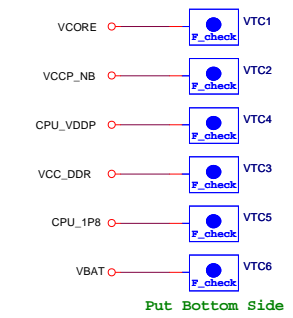
Voltage Mearsure Point



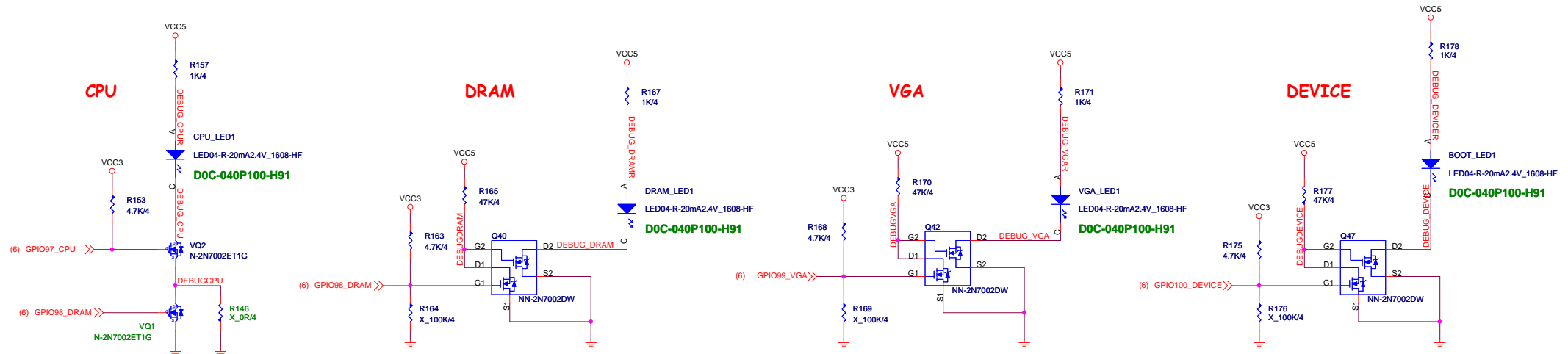
LED (for NCT6797D)



Factory check point



EZ Debug LED



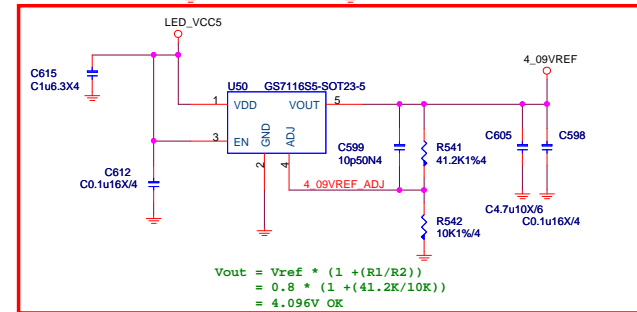
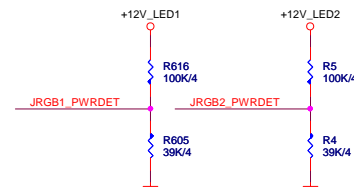
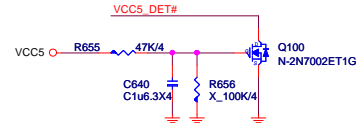
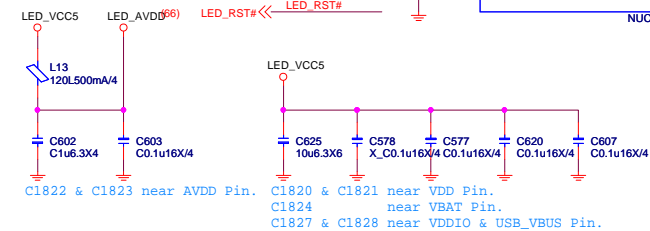
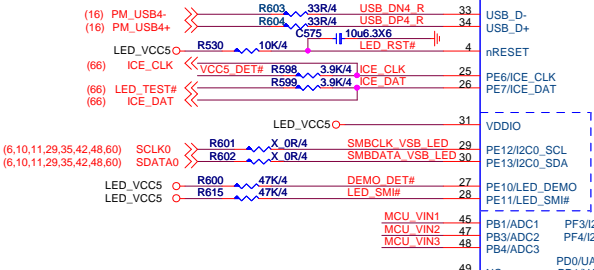
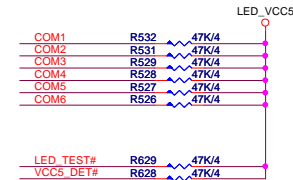
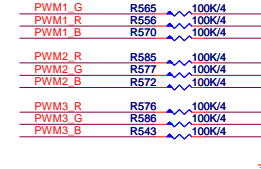
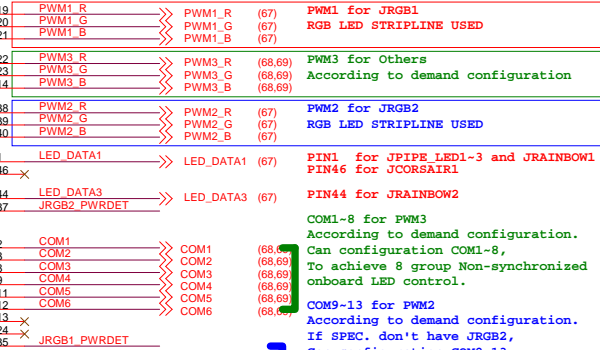
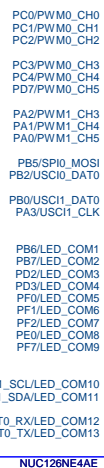
LED亮燈時同時將CPU LED關掉

LEDGPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

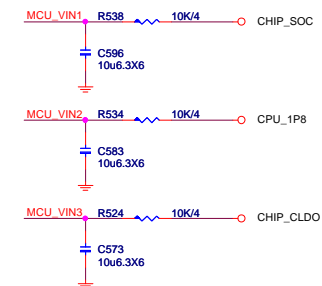
AMD AMP Detect LED

48 PIN LED MCU

If you use ADC function, need to separate VREF from AVDD and 4_09VREF stuff for VREF.



Option Spec For Voltage Monitor Require.



Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1-8	PWM3
Board Side LED	COM 9-13	PWM2



MICRO-STAR INT'L CO.,LTD

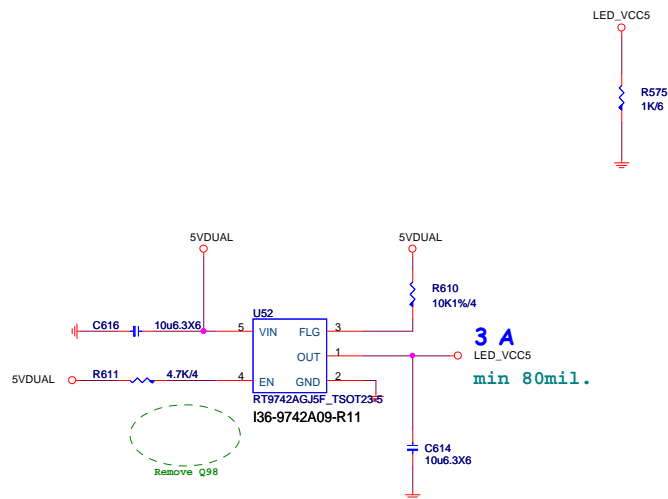
MS-7C37

Size	Document Description
Custom	MCU - LED Control

Rev
1.2

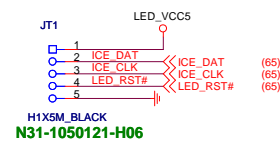
Date: Monday, April 01, 2019	Sheet 65 of 75
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EXTERNAL POWER INPUT

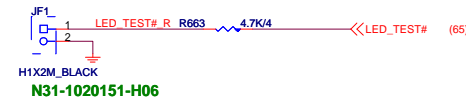


External Power

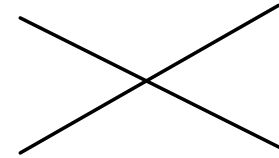
JT1 for FW update



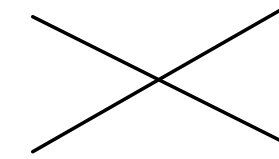
JF1 For Factory Test



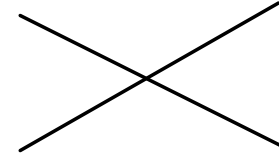
1 PCH HEATSINK LED



2 AUDIO/IO Cover LED



3 MOS HEATSINK LED



JPIPE:PIN1:output ,PIN2:input
PIN2:MCU IN
PIN1:HEATSINK OUT

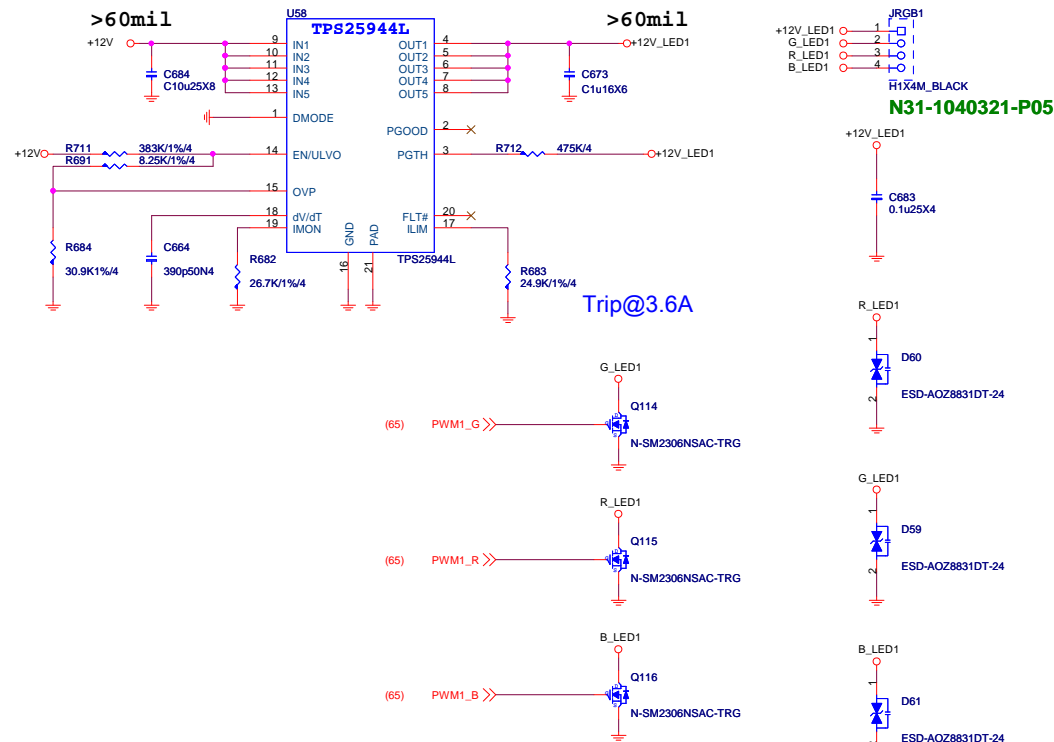


MICRO-STAR INT'L CO.,LTD

MS-7C37

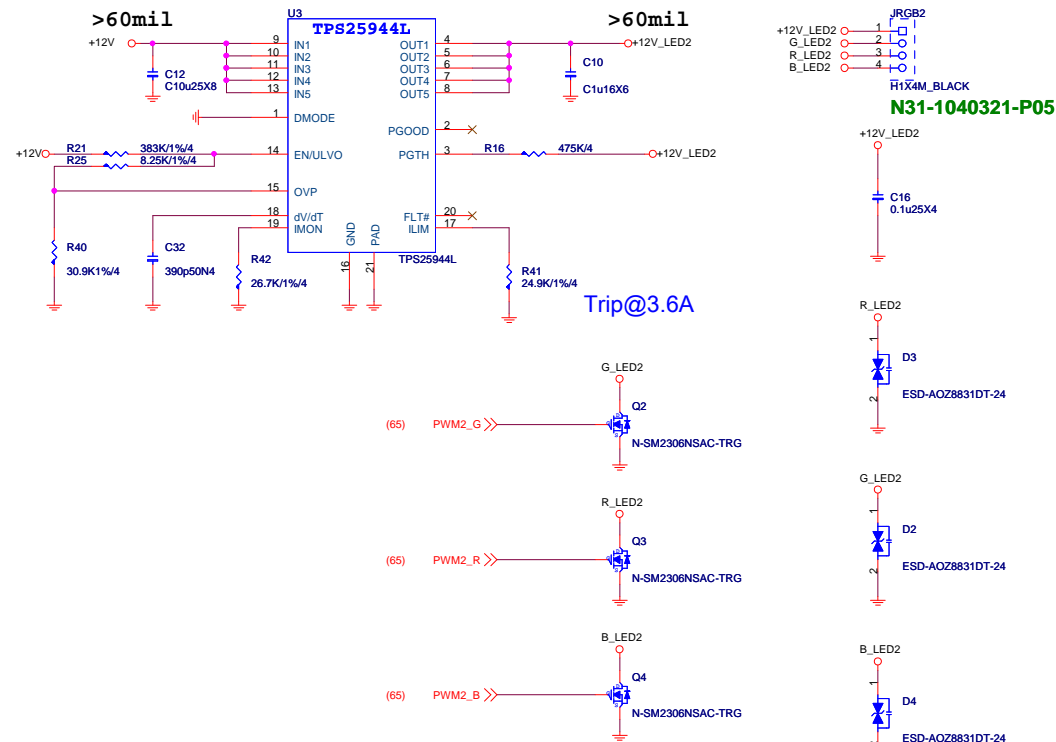
Size	Document Description	Rev
Custom	LED - Power / JPIPE	1.2
Date: Monday, April 01, 2019 Sheet 66 of 75		

JRGB1



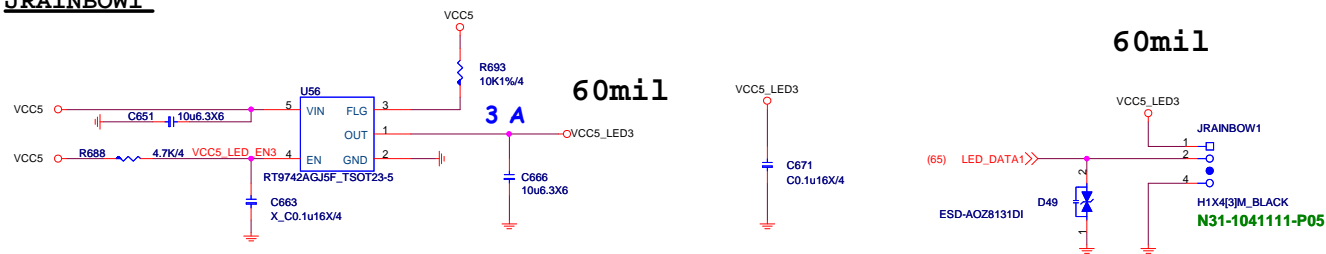
外接LED 燈條 (RGB)
 ---- PCB 文字面 (JRGB1)
 ---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JRGB2

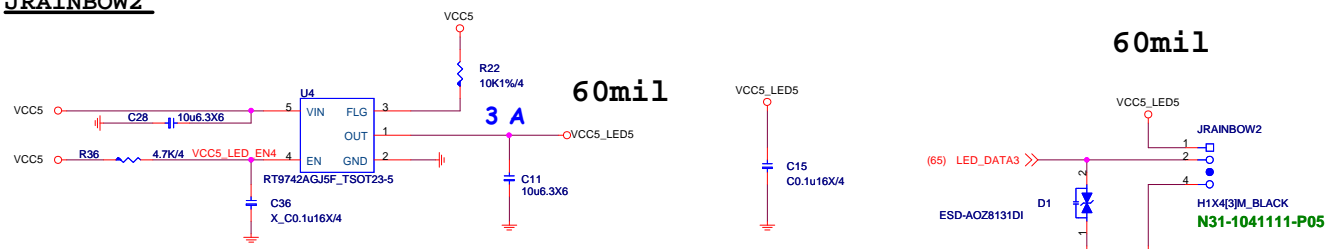


外接LED 燈條 (RGB)
 ---- PCB 文字面 (JRGB2)
 ---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

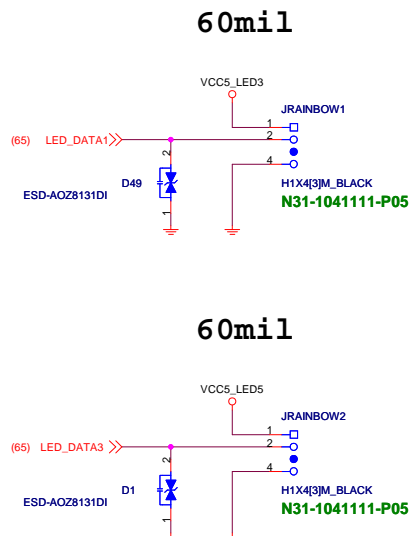
JRAINBOW1



JRAINBOW2

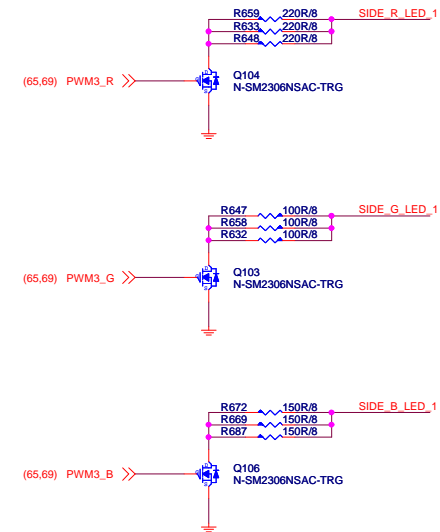
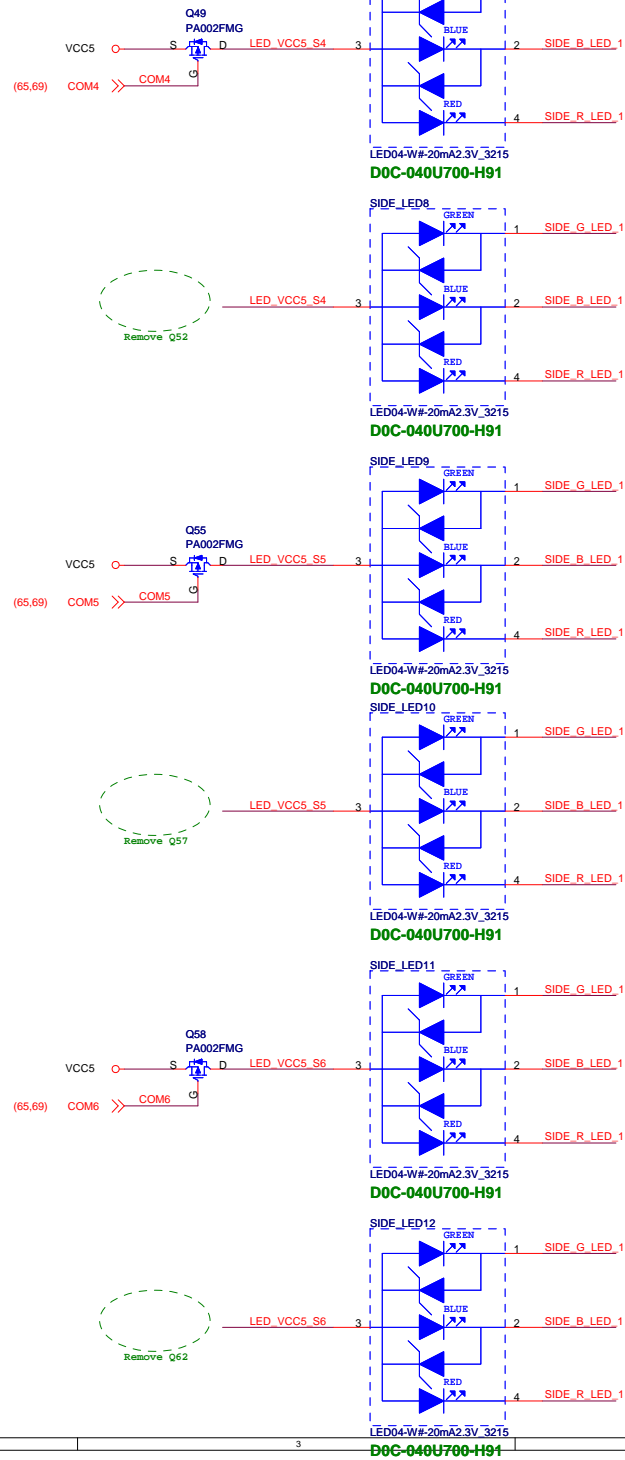
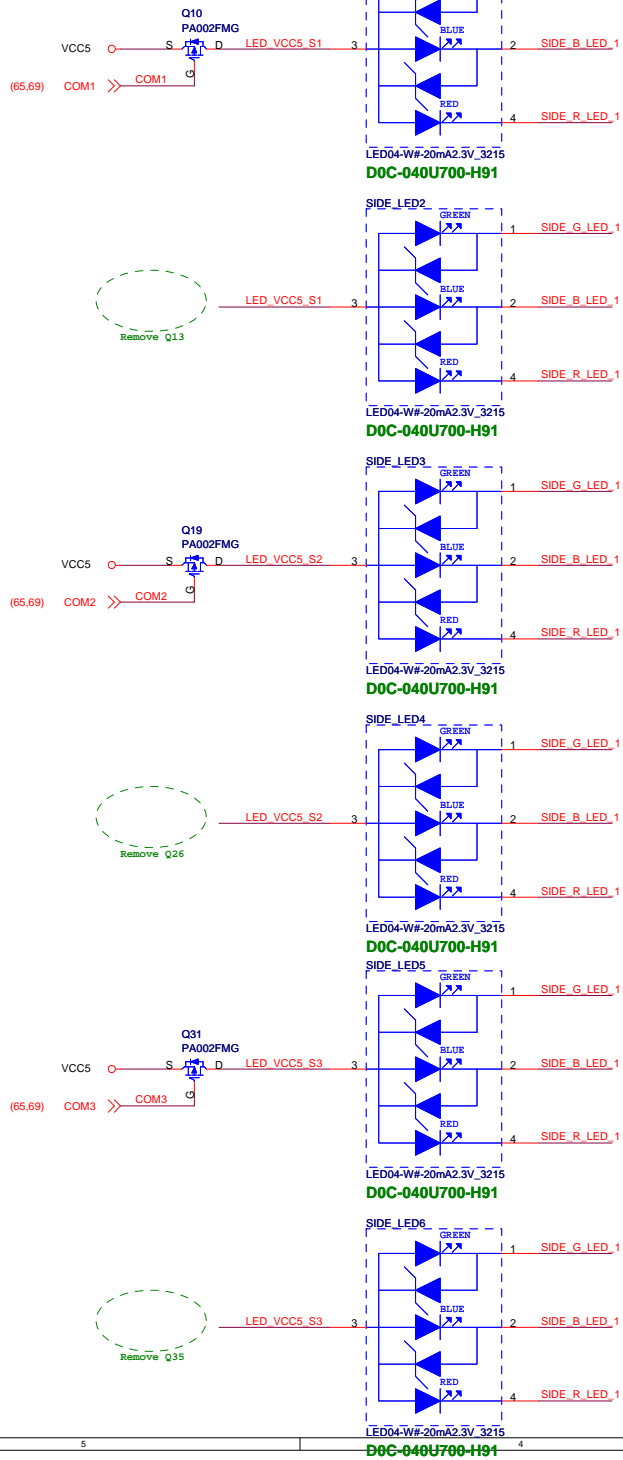


JCORSAIR1

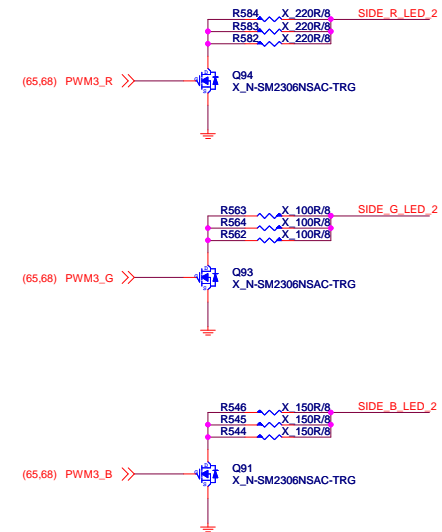
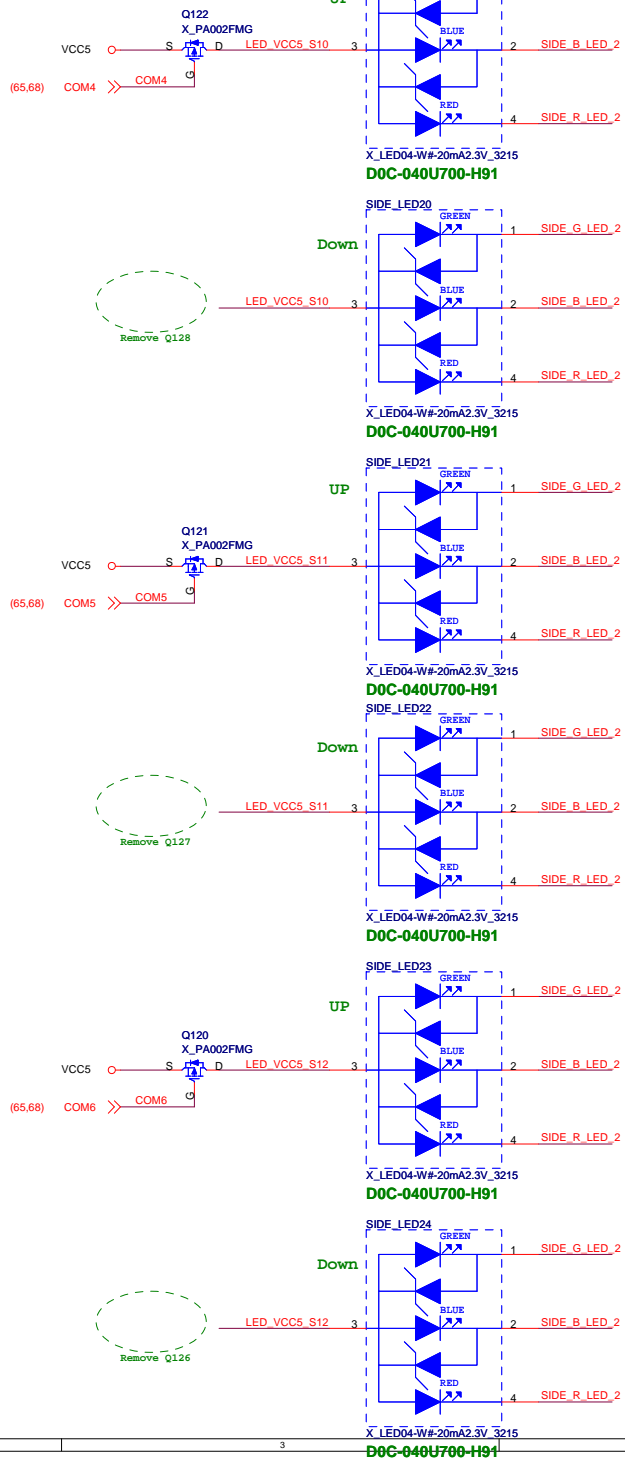
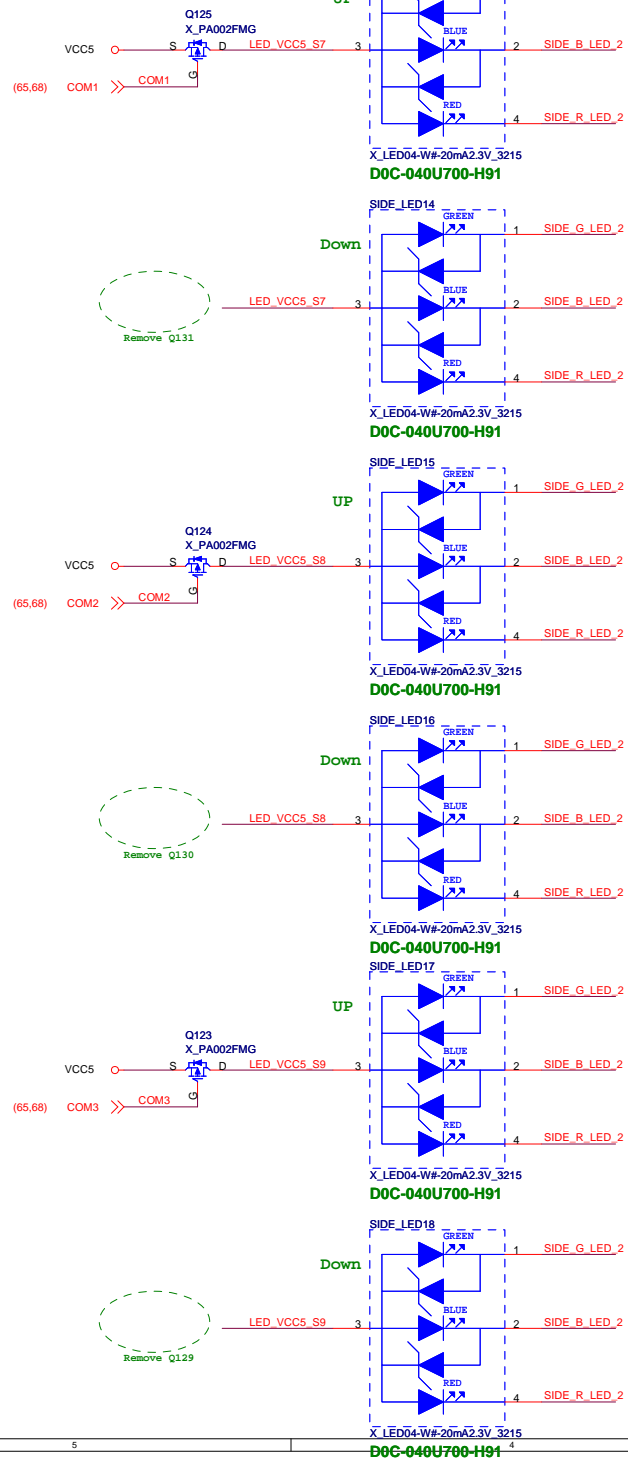


MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size Custom	Document Description	Rev 1.2
LED - JLED1 / 2 / 3 / 4		
Date: Monday, April 01, 2019	Sheet 67	of 75

Sidebar LED *12

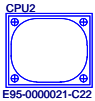


Market Name LED *12



	MICRO-STAR INT'L CO.,LTD		
	MS-7C37		
	Size Custom	Document Description LED - Market Name	Rev 1.2
Date: Monday, April 01, 2019			Sheet 69 of 75

CPU Socket



E95-0000022-C22

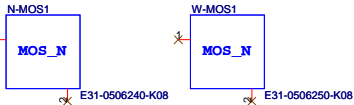
PCB

PCB1



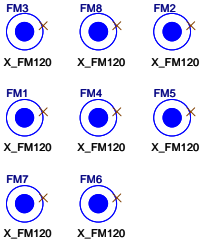
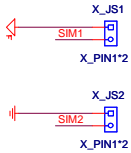
7C37-1.2
PD0-07C3712-E48

MOS HEATSINK

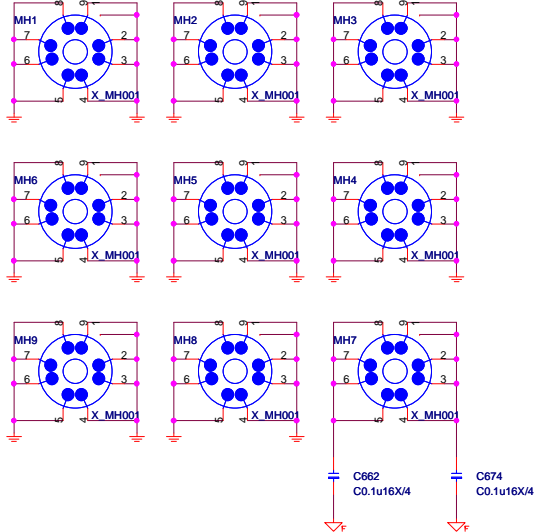


IO COVER

Simulation



Optics Orientation Holes



MANUAL PART

UEFI1
G51-M1SPXXA-A09
G51-M1SPXXA-A09

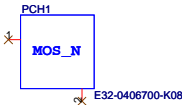
HDMI_LA1
Label
HDMI
HDMI LABEL
Y01-RHDMI03-000

NAHIMIC1
Y02-MU00100-NAH
Y02-MU00100-NAH

XSPILT1
X_Y02-MA00401-XSP
Y02-MA00401-XSP

SSE1
X_Y02-MA00101-SSE
Y02-MA00101-SSE

PCH HEATSINK



Audio COVER



DDR COVER